Group of 32-bit RISC processor cores "Bit-banding" redirects here. For the direct port bit software access method, see Bit-banging. For the construction of processors from n-bit-wide modules, see Bit-slicing. ARM Cortex-M0 and Cortex-M3 microcontroller ICs from NXP and Silicon Labs (Energy Micro) Die from a STM32F100C4T6B IC.24 MHz ARM Cortex-M3 microcontroller with 16 KB flash memory, 4 KB RAM. Manufactured by STMicroelectronics. The ARM Cortex-M is a group of 32-bit RISC ARM processor cores licensed by ARM Limited. These cores are optimized for low-cost and energy-efficient integrated circuits, which have been embedded in tens of billions of consumer devices.[1] Though they are most often the main component of microcontroller chips, sometimes they are embedded inside other types of chips too. The Cortex-M family consists of Cortex-M0,[2] Cortex-M0+,[3] Cortex-M1,[4] Cortex-M3,[5] Cortex-M4,[6] Cortex-M7,[7] Cortex-M23,[8] Cortex-M33,[9] Cortex-M35P,[10] Cortex-M52,[11] Cortex-M55,[12] Cortex-M85.[13] A floating-point unit (FPU) option is available for Cortex-M4 / M7 / M33 / M35P / M52 / M55 / M85 cores, and when included in the silicon these cores are sometimes known as "Cortex-MxF", where 'x' is the core variant. 32-bit Year Core 2004 Cortex-M3 2007 Cortex-M1 2009 Cortex-M0 2010 Cortex-M4 2012 Cortex-M0+ 2014 Cortex-M7 2016 Cortex-M23 2016 Cortex-M33 2018 Cortex-M35P 2020 Cortex-M55 2022 Cortex-M85 2023 Cortex-M52 See also: ARM architecture and List of ARM cores The ARM Cortex-M family are ARM microprocessor cores that are designed for use in microcontrollers, ASICs, ASSPs, FPGAs, and SoCs. Cortex-M cores are commonly used as dedicated microcontroller chips, but also are "hidden" inside of SoC chips as power management controllers, I/O controllers, system controllers, touch screen controllers, smart battery controllers, and sensor controllers. The main difference from Cortex-A cores is that Cortex-M cores have no memory management unit (MMU) for virtual memory, considered essential for "full-fledged" operating systems. Cortex-M programs instead run bare metal or on one of the many real-time operating systems which support a Cortex-M. Though 8-bit microcontrollers were very popular in the past, Cortex-M has slowly been chipping away at the 8-bit market as the prices of low-end Cortex-M chips have moved downward. Cortex-M have become a popular replacements for 8-bit chips in applications that benefit from 32-bit math operations, and replacing older legacy ARM cores such as ARM7 and ARM9. In particular, the embedded wear-leveling controller inside most SD cards or flash drives is a (8-bit) 8051 microcontroller or ARM CPU.[14] ARM Limited neither manufactures nor sells CPU devices based on its own designs, but rather licenses the processor architecture to interested parties. Arm offers a variety of licensing terms, varying in cost and deliverables. To all licensees, Arm provides an integratable hardware description of the ARM core, as well as complete software development toolset and the right to sell manufactured silicon containing the ARM CPU. Integrated Device Manufacturers (IDM) receive the ARM Processor IP as synthesizable RTL (written in Verilog). In this form, they have the ability to perform architectural level optimizations and extensions. This allows the manufacturer to achieve custom design goals, such as higher clock speed, very low power consumption, instruction set extensions (including floating point), optimizations for size, debug support, etc. To determine which components have been included in a particular ARM CPU chip, consult the manufacturer datasheet and related documentation. Some of the silicon options for the Cortex-M cores are: SysTick timer: A 24-bit system timer that extends the functionality of both the processor and the Nested Vectored Interrupt Controller (NVIC). When present, it also provides an additional configurable priority SysTick interrupt.[15][16][17] Though the SysTick timer is optional for the M0/M0+/M1/M23, it is extremely rare to find a Cortex-M microcontroller without it. If a Cortex-M33/M35P/M52/M55/M85 microcontroller has the Security Extension option, then it optionally can have two SysTicks (one Secure, one Non-secure). Bit-Band: Maps a complete word of memory onto a single bit in the bit-band region. For example, writing to an alias word will set or clear the corresponding bit in the bit-band region. This allows every individual bit in the bit-band region to be directly accessible from a word-aligned address. In particular, individual bits can be set, cleared, or toggled from C/C++ without performing a read-modify-write sequence of instructions.[15][16][17] Though the bit-band is optional, it is less common to find a Cortex-M3 and Cortex-M4 microcontroller without it. Some Cortex-M0 and Cortex-M0+ microcontrollers have bit-band. Memory Protection Unit (MPU): Provides support for protecting regions of memory through enforcing privilege and access rules. It supports up to sixteen different regions, each of which can be split further into equal-size sub-regions.[15][16][17] Tightly-Coupled Memory (TCM): Low-latency (zero wait state) SRAM that can be used to hold the call stack, RTOS control structures, interrupt data structures, interrupt handler code, and speed critical code. Other than CPU cache, TCM is the fastest memory in an ARM Cortex-M microcontroller. Since TCM isn't cached and accessible at the same speed as the processor and cache, it could be conceptually described as "addressable cache". There is an ITCM (Instruction TCM) and a DTCM (Data TCM) to allow a Harvard architecture processor to read from both simultaneously. The DTCM can't contain any instructions, but the ITCM can contain data. Since TCM is tightly connected to the processor core, DMA engines might not be able to access TCM on some implementations. ARM Cortex-M optional components ARM Core CortexM0[18] CortexM0+[19] CortexM1[20] CortexM3[21] CortexM4[22] CortexM7[23] CortexM23[24] CortexM33[25] CortexM35P[10] CortexM52[26] CortexM55[27] CortexM85[28] SysTick 24-bit Timer Optional(0,1) Optional(0, 1) Optional(0,1) Yes(1) Yes(1) Yes(1) Optional(0, 1, 2) Yes(1, 2) Yes(1, 2) Yes(1, 2) Yes(1, 2) Yes(1, 2) Single-cycle I/O port No Optional No No No No Optional No No No No No Bit-Band memory No[29] No[29] No* Optional Optional Optional No No No No No No Memory ProtectionUnit (MPU) No Optional(0, 8) No Optional(0,8) Optional(0, 8) Optional(0, 8, 16) Optional(0, 4, 8, 12, 16) Optional(0, 4, 8, 12, 16) Optional(up to 16)* Optional(0, 4, 8, 12, 16) Optional(0, 4, 8, 12, 16) Optional(0, 4, 8, 12, 16) Security AttributionUnit (SAU) andStack Limits No No No No No No Optional(0, 4, 8) Optional(0, 4, 8) Optional(up to 8)* Optional(0, 4, 8) Optional(0, 4, 8) Optional(0, 4, 8) Instruction Cache No[30] No[30] No[30] No[30] No[30] Optional(up to 64 KB) No No Optional(up to 16 KB) Optional(up to 64 KB) Optional(up to 64 KB) Optional(up to 64 KB) Data Cache No[30] No[30] No[30] No[30] No[30] Optional(up to 64 KB) No No Optional(up to 16 KB) Optional(up to 64 KB) Optional(up to 64 KB) Optional(up to 64 KB) Instruction TCM(ITCM) Memory No No Optional(up to 1 MB) No No Optional(up to 16 MB) No No No Optional(up to 16 MB) Optional(up to 16 MB) Optional(up to 16 MB) Data TCM(DTCM) Memory No No Optional(up to 1 MB) No No Optional(up to 16 MB) No No No Optional(up to 16 MB) Optional(up to 16 MB) Optional(up to 16 MB) ECC for TCMand Cache No No No No No No No No Optional Optional Optional Optional Vector Table OffsetRegister (VTOR) No Optional(0,1) Optional(0,1) Optional(0,1) Optional(0,1) Optional(0,1) Optional(0,1,2) Yes(1,2) Yes(1,2) Yes(1,2) Yes(1,2) Yes(1,2) Note: Most Cortex-M3 and M4 chips have bit-band and MPU. The bit-band option can be added to the M0/M0+ using the Cortex-M System Design Kit.[29] Note: Software should validate the existence of each feature before attempting to use it.[17] Note: Limited public information is available for the Cortex-M35P until its Technical Reference Manual is released. Additional silicon options:[15][16] Data endianness: Little-endian or big-endian. Unlike legacy ARM cores, the Cortex-M is permanently fixed in silicon as one of these choices. Interrupts: 1 to 32 (M0/M0+/M1), 1 to 240 (M3/M4/M7/M23), 1 to 480 (M33/M35P/M52/M55/M85). Wake-up interrupt controller: Optional. Vector Table Offset Register: Optional. (not available for M0). Instruction fetch width: 16-bit only, or mostly 32-bit. User/privilege support: Optional. Reset all registers: Optional. Single-cycle I/O port: Optional. (M0+/M23). Debug Access Port (DAP): None, SWD, JTAG and SWD. (optional for all Cortex-M cores) Halting debug support: Optional. Number of watchpoint comparators: 0 to 2 (M0/M0+/M1), 0 to 4 (M3/M4/M7/M23/M33/M35P/M52/M55/M85). Number of breakpoint comparators: 0 to 4 (M0/M0+/M1/M23), 0 to 8 (M3/M4/M7/M33/M35P/M52/M55/M85). See also: ARM architecture § Instruction set The Cortex-M0 / M0+ / M1 implement the ARMv6-M architecture,[15] the Cortex-M3 implements the ARMv7-M architecture,[16] the Cortex-M4 / Cortex-M7 implements the ARMv7E-M architecture,[16] the Cortex-M23 / M33 / M35P implement the ARMv8-M architecture,[31] and the Cortex-M52 / M55 / M85 implements the ARMv8.1-M architecture.[31] The architectures are binary instruction upward compatible from ARMv6-M to ARMv7-M to ARMv7E-M. Binary instructions available for the Cortex-M0 / Cortex-M0+ / Cortex-M1 can execute without modification on the Cortex-M3 / Cortex-M4 / Cortex-M7. Binary instructions available for the Cortex-M3 can execute without modification on the Cortex-M4 / Cortex-M7 / Cortex-M33 / Cortex-M35P.[15][16] Only Thumb-1 and Thumb-2 instruction sets are supported in Cortex-M architectures; the legacy 32-bit ARM instruction set isn't supported. All Cortex-M cores implement a common subset of instructions that consists of most Thumb-1, some Thumb-2, including a 32-bit result multiply. The Cortex-M0 / Cortex-M0+ / Cortex-M1 / Cortex-M23 were designed to create the smallest silicon die, thus having the fewest instructions of the Cortex-M family. The Cortex-M0 / M0+ / M1 include Thumb-1 instructions, except new instructions (CBZ, CBNZ, IT) which were added in ARMv7-M architecture. The Cortex-M0 / M0+ / M1 include a minor subset of Thumb-2 instructions (BL, DMB, DSB, ISB, MRS, MSR).[15] The Cortex-M3 / M4 / M7 / M33 / M35P have all base Thumb-1 and Thumb-2 instructions. The Cortex-M3 adds three Thumb-1 instructions, all Thumb-2 instructions, hardware integer divide, and saturation arithmetic instructions. The Cortex-M4 adds DSP instructions and an optional single-precision floating-point unit (VFPv4-SP). The Cortex-M7 adds an optional double-precision FPU (VFPv5).[23][16] The Cortex-M23 / M33 / M35P / M52 / M55 / M85 add TrustZone instructions. ARM Cortex-M instruction variations Arm Core CortexM0[18] CortexM0+[19] CortexM1[20] CortexM3[21] CortexM4[22] CortexM7[23] CortexM23[24] CortexM33[25] CortexM35P CortexM52[26] CortexM55[27] CortexM85[28] ARM architecture ARMv6-M[15] ARMv6-M[15] ARMv6-M[15] ARMv7-M[16] ARMv7E-M[16] ARMv7E-M[16] ARMv8-MBaseline[31] ARMv8-MMainline[31] ARMv8-MMainline[31] Armv8.1-MMainline[31] Armv8.1-MMainline[31] Armv8.1-MMainline[31] Computer architecture VonNeumann VonNeumann VonNeumann Harvard Harvard Harvard VonNeumann Harvard Harvard Harvard Harvard Harvard Instruction pipeline 3 stages 2 stages 3 stages 3 stages 3 stages 6 stages 2 stages 3 stages 3 stages 4 stages 4-5 stages 7 stages Interrupt latency(zero wait state memory) 16 cycles 15 cycles 23 for NMI,26 for IRQ 12 cycles 12 cycles 12 cycles,14 worstcase 15 cycles,24 secureto NS IRQ 12 cycles,21 secureto NS IRQ TBD TBD TBD TBD Thumb-1 instructions Most Most Most Entire Entire Entire Most Entire Entire Entire Entire Entire Thumb-2 instructions Some Some Some Entire Entire Entire Some Entire Entire Entire Entire Entire Multiply instructions32×32 = 32-bit result Yes Yes Yes Yes Yes Yes Yes Yes Yes Yes Yes Yes Multiply instructions32×32 = 64-bit result No No No Yes Yes Yes No Yes Yes Yes Yes Yes Divide instructions32/32 = 32-bit quotient No No No Yes Yes Yes Yes Yes Yes Yes Yes Yes Saturated math instructions No No No Some Yes Yes No Yes Yes Yes Yes Yes DSP instructions No No No No Yes Yes No Optional Optional Yes Yes Yes Half-Precision (HP)floating-point instructions No No No No No No No No No Optional Optional Optional Single-Precision (SP)floating-point instructions No No No No Optional Optional No Optional Optional Optional Optional Optional Double-Precision (DP)floating-point instructions No No No No No Optional No No No Optional Optional Optional Helium vector instructions No No No No No No No No No Optional Optional Optional TrustZone security instructions No No No No No No Optional Optional Optional Optional Optional Yes Co-processor instructions No No No No No No No Optional Optional Optional Optional Optional ARM Custom Instructions (ACI) No No No No No No No Optional No Optional Optional Optional Pointer Authentication and Branch TargetIdentification (PACBTI) instructions No No No No No No No No No Optional No Optional Note: Interrupt latency cycle count assumes: 1) stack located in zero-wait state RAM, 2) another interrupt function not currently executing, 3) Security Extension option doesn't exist, because it adds additional cycles. The Cortex-M cores with a Harvard computer architecture have a shorter interrupt latency than Cortex-M cores with a Von Neumann computer architecture. Note: The Cortex-M series includes three new 16-bit Thumb-1 instructions for sleep mode: SEV, WFE, WFI. Note: The Cortex-M0 / M0+ / M1 doesn't include these 16-bit Thumb-1 instructions: CBZ, CBNZ, IT.[15][16] Note: The Cortex-M0 / M0+ / M1 only include these 32-bit Thumb-2 instructions: BL, DMB, DSB, ISB, MRS, MSR.[15][16] Note: The Cortex-M0 / M0+ / M1 / M23 only has 32-bit multiply instructions with a lower-32-bit result (32 bit × 32 bit = lower 32 bit), where as the Cortex-M3 / M4 / M7 / M33 / M35P includes additional 32-bit multiply instructions with 64-bit results (32 bit × 32 bit = 64 bit). The Cortex-M4 / M7 (optionally M33 / M35P) include DSP instructions for (16 bit × 16 bit = 32 bit), (32 bit × 16 bit = upper 32 bit), (32 bit × 32 bit = upper 32 bit) multiplications.[15][16] Note: The number of cycles to complete multiply and divide instructions vary across ARM Cortex-M core designs. Some cores have a silicon option for the choice of fast speed or small size (slow speed), so cores have the option of using less silicon with the downside of higher cycle count. An interrupt occurring during the execution of a divide instruction or slow-iterative multiply instruction will cause the processor to abandon the instruction, then restart it after the interrupt returns. Multiply instructions "32-bit result" – Cortex-M0/M0+/M23 is 1 or 32 cycle silicon option, Cortex-M1 is 3 or 33 cycle silicon option, Cortex-M3/M4/M7/M33/M35P is 1 cycle. Multiply instructions "64-bit result" – Cortex-M3 is 3–5 cycles (depending on values), Cortex-M4/M7/M33/M35P is 1 cycle. Divide instructions – Cortex-M3/M4 is 2–12 cycles (depending on values), Cortex-M7 is 3–20 cycles (depending on values), Cortex-M23 is 17 or 34 cycle option, Cortex-M33 is 2–11 cycles (depending on values), Cortex-M35P is TBD. Note: Some Cortex-M cores have silicon options for various types of floating point units (FPU). The Cortex-M55 / M85 has an option for half-precision (HP), the Cortex-M4 / M7 / M33 / M35P / M52 / M55 / M85 has an option for single-precision (SP), the Cortex-M7 / M52 / M55 / M85 has an option for double-precision (DP). When an FPU is included, the core is sometimes referred as "Cortex-MxF", where 'x' is the core variant, such as Cortex-M4F. [15][16] ARM Cortex-M instruction groups Group Instrbits Instructions CortexM0, M0+, M1 CortexM3 CortexM4 CortexM7 CortexM23 CortexM33 CortexM35P CortexM52 CortexM55 CortexM85 Thumb-1 16 ADC, ADD, ADR, AND, ASR, B, BIC, BKPT, BLX, BX, CMN, CMP, CPS, EOR, LDM, LDR, LDRB, LDRH, LDRSB, LDRSH, LSL, LSR, MOV, MUL, MVN, NOP, ORR, POP, PUSH, REV, REV16, REVSH, ROR, RSB, SBC, SEV, STM, STR, STRB, STRH, SUB, SVC, SXTB, SXTH, TST, UXTB, UXTH, WFE, WFI, YIELD Yes Yes Yes Yes Yes Yes Yes Yes Yes Yes Thumb-1 16 CBNZ, CBZ No Yes Yes Yes Yes Yes Yes Yes Yes Yes Thumb-1 16 IT No Yes Yes Yes No Yes Yes Yes Yes Yes Thumb-2 32 BL, DMB, DSB, ISB, MRS, MSR Yes Yes Yes Yes Yes Yes Yes Yes Yes Yes Thumb-2 32 SDIV, UDIV, MOVT, MOVW, B.W, LDREX, LDREXB, LDREXH, STREX, STREXB, STREXH No Yes Yes Yes Yes Yes Yes Yes Yes Yes Thumb-2 32 ADC, ADD, ADR, AND, ASR, B, BFC, BFI, BIC, CDP, CLREX, CLZ, CMN, CMP, DBG, EOR, LDC, LDM, LDR, LDRB, LDRBT, LDRD, LDRH, LDRHT, LDRSB, LDRSBT, LDRSH, LDRSHT, LDRT, LSL, LSR, MCR, MCRR, MLA, MLS, MRC, MRRC, MUL, MVN, NOP, ORN, ORR, PLD, PLDW, PLI, POP, PUSH, RBIT, REV, REV16, REVSH, ROR, RRX, RSB, SBC, SBFX, SEV, SMLAL, SMULL, SSAT, STC, STM, STR, STRB, STRBT, STRD, STRH, STRHT, STRT, SUB, SXTB, SXTH, TBB, TBH, TEQ, TST, UBFX, UMLAL, UMULL, USAT, UXTB, UXTH, WFE, WFI, YIELD No Yes Yes Yes No Yes Yes Yes Yes Yes DSP 32 PKH, QADD, QADD16, QADD8, QASX, QDADD, QDSUB, QSAX, QSUB, QSUB16, QSUB8, SADD16, SADD8, SASX, SEL, SHADD16, SHADD8, SHASX, SHSAX, SHSUB16, SHSUB8, SMLABB, SMLABT, SMLATB, SMLATT, SMLAD, SMLALBB, SMLALBT, SMLALTB, SMLALTT, SMLALD, SMLAWB, SMLAWT, SMLSD, SMLSLD, SMMLA, SMMLS, SMMUL, SMUAD, SMULBB, SMULBT, SMULTT, SMULTB, SMULWT, SMULWB, SMUSD, SSAT16, SSAX, SSUB16, SSUB8, SXTAB, SXTAB16, SXTAH, SXTB16, UADD16, UADD8, UASX, UHADD16, UHADD8, UHASX, UHSAX, UHSUB16, UHSUB8, UMAAL, UQADD16, UQADD8, UQASX, UQSAX, UQSUB16, UQSUB8, USAD8, USADA8, USAT16, USAX, USUB16, USUB8, UXTAB, UXTAB16, UXTAH, UXTB16 No No Yes Yes No Optional Optional Yes Yes Yes SP Float 32 VABS, VADD, VCMP, VCMPE, VCVT, VCVTR, VDIV, VLDM, VLDR, VMLA, VMLS, VMOV, VMRS, VMSR, VMUL, VNEG, VNMLA, VNMLS, VNMUL, VPOP, VPUSH, VSQRT, VSTM, VSTR, VSUB No No Optional Optional No Optional Optional Optional Optional Optional DP Float 32 VCVTA, VCVTM, VCVTN, VCVTP, VMAXNM, VMINNM, VRINTA, VRINTM, VRINTN, VRINTP, VRINTR, VRINTX, VRINTZ, VSEL No No No Optional No No No Optional Optional Optional Acquire/Release 32 LDA, LDAB, LDAH, LDAEX, LDAEXB, LDAEXH, STL, STLB, STLH, STLEX, STLEXB, STLEXH No No No No Yes Yes Yes Yes Yes Yes TrustZone 16 BLXNS, BXNS No No No No Optional Optional Optional Optional Optional Yes 32 SG, TT, TTT, TTA, TTAT Co-processor 16 CDP, CDP2, MCR, MCR2, MCRR, MCRR2, MRC, MRC2, MRRC, MRRC2 No No No No No Optional Optional Optional Optional Optional ACI 32 CX1, CX1A, CX2, CX2A, CX3, CX3A, CX1D, CX1DA, CX2D, CX2DA, CX3D, CX3DA, VCX1, VCX1A, VCX2, VCX2A, VCX3, VCX3A No No No No No Optional No Optional Optional Optional PACBTI 32 AUT, AUTG, BTI, BXAUT, PAC, PACBTI, PACG No No No No No No No Optional No Optional Note: MOVW is an alias that means 32-bit "wide" MOV instruction. Note: B.W is a long-distance unconditional branch (similar in encoding, operation, and range to BL, minus setting of the LR register). Note: For Cortex-M1, WFE / WFI / SEV instructions exist, but execute as a NOP instruction. Note: The half-precision (HP) FPU instructions are valid in the Cortex-M52 / M55 / M85 only when the HP FPU option exists in the silicon. Note: The single-precision (SP) FPU instructions are valid in the Cortex-M4 / M7 / M33 / M35P / M52 / M55 / M85 only when the SP FPU option exists in the silicon. Note: The double-precision (DP) FPU instructions are valid in the Cortex-M7 / M52 / M55 / M85 only when the DP FPU option exists in the silicon. The ARM architecture for ARM Cortex-M series removed some features from older legacy cores:[15][16] The 32-bit ARM instruction set is not included in Cortex-M cores. Endianness is chosen at silicon implementation in Cortex-M cores. Legacy cores allowed "on-the-fly" changing of the data endian mode. Co-processors were not supported on Cortex-M cores, until the silicon option was reintroduced in "ARMv8-M Mainline" for ARM Cortex-M33/M35P cores. The capabilities of the 32-bit ARM instruction set is duplicated in many ways by the Thumb-1 and Thumb-2 instruction sets, but some ARM features don't have a similar feature: The SWP and SWPB (swap) ARM instructions don't have a similar feature in Cortex-M. The 16-bit Thumb-1 instruction set has evolved over time since it was first released in the legacy ARM7T cores with the ARMv4T architecture. New Thumb-1 instructions were added as each legacy ARMv5 / ARMv6 / ARMv6T2 architectures were released. Some 16-bit Thumb-1 instructions were removed from the Cortex-M cores: The "BLX " instruction doesn't exist because it was used to switch from Thumb-1 to ARM instruction set. The "BLX " instruction is still available in the Cortex-M. SETEND doesn't exist because on-the-fly switching of data endian mode is no longer supported. Co-processor instructions were not supported on Cortex-M cores, until the silicon option was reintroduced in "ARMv8-M Mainline" for ARM Cortex-M33/M35P cores. The SWI instruction was renamed to SVC, though the instruction binary coding is the same. However, the SVC handler code is different from the SWI handler code, because of changes to the exception models. Cortex-M0Architecture and classificationInstruction setARMv6-M (Thumb-1 (most),Thumb-2 (some)) The Cortex-M0 core is optimized for small silicon die size and use in the lowest price chips.[2] Key features of the Cortex-M0 core are:[18] ARMv6-M architecture[15] 3-stage pipeline Instruction sets: Thumb-1 (most), missing CBZ, CBNZ, IT Thumb-2 (some), only BL, DMB, DSB, ISB, MRS, MSR 32-bit hardware integer multiply with 32-bit result 1 to 32 interrupts, plus NMI Silicon options: Hardware integer multiply speed: 1 or 32 cycles. nRF51822 The following microcontrollers are based on the Cortex-M0 core: ABOV AC30M1x64 Cypress PSoC 4000, 4100, 4100M, 4200, 4200DS, 4200L, 4200M Infineon XMC1100, XMC1200, XMC1300, XMC1400, TLE984x Dialog DA1458x, DA1468x Nordic nRF51 NXP LPC1100, LPC1200 Nuvoton NuMicro Sonix SN32F700 ST STM32 F0 Toshiba TX00 Vorago VA10800 (extreme temperature), VA10820 (radiation hardened) The following chips have a Cortex-M0 as a secondary core: NXP LPC4300 (one Cortex-M4F + one Cortex-M0) Texas Instruments SimpleLink Wireless MCUs CC1310 and CC2650 (one programmable Cortex-M3 + one Cortex-M0 network processor + one proprietary Sensor Controller Engine) Cortex-M0+Architecture and classificationMicroarchitectureARMv6-MInstruction setThumb-1 (most),Thumb-2 (some) NXP (Freescale) FRDM-KL25Z Board with KL25Z128VLK (Kinetis L) The Cortex-M0+ is an optimized superset of the Cortex-M0. The Cortex-M0+ has complete instruction set compatibility with the Cortex-M0 thus allowing the use of the same compiler and debug tools. The Cortex-M0+ pipeline was reduced from 3 to 2 stages, which lowers the power usage and increases performance (higher average IPC due to branches taking one fewer cycle). In addition to debug features in the existing Cortex-M0, a silicon option can be added to the Cortex-M0+ called the Micro Trace Buffer (MTB) which provides a simple instruction trace buffer. The Cortex-M0+ also received Cortex-M3 and Cortex-M4 features, which can be added as silicon options, such as the memory protection unit (MPU) and the vector table relocation.[19] Key features of the Cortex-M0+ core are:[19] ARMv6-M architecture[15] 2-stage pipeline (one fewer than Cortex-M0) Instruction sets: (same as Cortex-M0) Thumb-1 (most), missing CBZ, CBNZ, IT Thumb-2 (some), only BL, DMB, DSB, ISB, MRS, MSR 32-bit hardware integer multiply with 32-bit result 1 to 32 interrupts, plus NMI Silicon options: Hardware integer multiply speed: 1 or 32 cycles 8-region memory protection unit (MPU) (same as M3 and M4) Vector table relocation (same as M3, M4) Single-cycle I/O port (available in M0+/M23) Micro Trace Buffer (MTB) (available in M0+/M23/M33/M35P) The following microcontrollers are based on the Cortex-M0+ core: ABOV Semiconductor A31G11x, A31G12x, A31G314 Cypress PSoC 4000S, 4100S, 4100S+, 4100PS, 4700S, FM0+ Epson S1C31W74, S1C31D01, S1C31D50 Holtek HT32F52000 Microchip SAM C2, D0, D1, D2, DA, L2, R2, R3; and PIC32CM JH and MC[32] NXP LPC800, LPC11E60, LPC11U60 NXP (Freescale) Kinetis E, EA, L, M, V1, W0, S32K11x Raspberry Pi RP2040 (two M0+ cores) Renesas S124, S128, RE, RE01 Silicon Labs (Energy Micro) EFM32 Zero, Happy ST STM32 L0, G0, C0, WL (one Cortex-M4 + one Cortex-M0+) The following chips have a Cortex-M0+ as a secondary core: Cypress PSoC 6200 (one Cortex-M4F + one Cortex-M0+) ST WB (one Cortex-M4F + one Cortex-M0+) The smallest ARM microcontrollers are of the Cortex-M0+ type (as of 2014, smallest at 1.6 mm by 2 mm in a chip-scale package is Kinetis KL03).[33] On 21 June 2018, the "world's smallest computer'", or computer device was announced – based on the ARM Cortex-M0+ (and including RAM and wireless transmitters and receivers based on photovoltaics) – by University of Michigan researchers at the 2018 Symposia on VLSI Technology and Circuits with the paper "A 0.04mm3 16nW Wireless and Batteryless Sensor System with Integrated Cortex-M0+ Processor and Optical Communication for Cellular Temperature Measurement." The device is one-tenth the size of IBM's previously claimed world-record-sized computer from months back in March 2018, which is smaller than a grain of salt. Cortex-M1Architecture and classificationMicroarchitectureARMv6-MInstruction setThumb-1 (most),Thumb-2 (some) The Cortex-M1 is an optimized core especially designed to be loaded into FPGA chips.[4] Key features of the Cortex-M1 core are:[20] ARMv6-M architecture[15] 3-stage pipeline. Instruction sets: Thumb-1 (most), missing CBZ, CBNZ, IT. Thumb-2 (some), only BL, DMB, DSB, ISB, MRS, MSR. 32-bit hardware integer multiply with 32-bit result. 1 to 32 interrupts, plus NMI. Silicon options: Hardware integer multiply speed: 3 or 33 cycles. Optional Tightly-Coupled Memory (TCM): 0 to 1 MB instruction-TCM, 0 to 1 MB data-TCM, each with optional ECC. External interrupts: 0, 1, 8, 16, 32. Debug: none, reduced, full. Data endianness: little-endian or BE-8 big-endian. OS extension: present or absent. The following vendors support the Cortex-M1 as soft-cores on their FPGA chips: Altera Cyclone-II, Cyclone-III, Stratix-II, Stratix-III GOWIN M1[34] Actel/Microsemi/Microchip Fusion, IGLOO/e, ProASIC3L, ProASIC3/E Xilinx Spartan-3, Virtex-2, Virtex-3, Virtex-4, Artix-7[35] Cortex-M3Architecture and classificationMicroarchitectureARMv7-MInstruction setThumb-1, Thumb-2, Saturated (some), Divide Arduino Due board with Atmel ATSAM3X8E (ARM Cortex-M3 core) microcontroller NXP LPCXpresso Development Board with LPC1343 Key features of the Cortex-M3 core are:[21][36] ARMv7-M architecture[16] 3-stage pipeline with branch speculation. Instruction sets: Thumb-1 (entire). Thumb-2 (entire). 32-bit hardware integer multiply with 32-bit or 64-bit result, signed or unsigned, add or subtract after the multiply. 32-bit multiply is 1 cycle, but 64-bit multiply and MAC instructions require extra cycles. 32-bit hardware integer divide (2–12 cycles). saturation arithmetic support. 1 to 240 interrupts, plus NMI. 12 cycle interrupt latency. Integrated sleep modes. Silicon options: Optional Memory Protection Unit (MPU): 0 or 8 regions. The following microcontrollers are based on the Cortex-M3 core: ABOV AC33Mx128, AC33Mx064 Actel/Microsemi/Microchip SmartFusion, SmartFusion 2 (FPGA) Analog Devices ADUCM360, ADUCM361, ADUCM3029 Broadcom Wi-Fi Chip BCM4319XKUBG Cypress PSoC 5000, 5000LP, FM3 Holtek HT32F Infineon TLE9860, TLE987x Microchip (Atmel) SAM 3A, 3N, 3S, 3U, 3X NXP LPC1300, LPC1700, LPC1800 ON Q32M210 Realtek RTL8710 Silicon Labs Precision32 Silicon Labs (Energy Micro) EFM32 Tiny, Gecko, Leopard, Giant ST STM32 F1, F2, L1, W TDK-Micronas HVC4223F Texas Instruments F28, LM3, TMS470, OMAP 4, SimpleLink Wireless MCUs (CC1310 Sub-GHz and CC2650 BLE+Zigbee+6LoWPAN) Toshiba TX03 mindmotion mindmotion MM32 The following chips have a Cortex-M3 as a secondary core: Apple A9 (Cortex-M3 as integrated M9 motion co-processor) CSR Quatro 5300 (Cortex-M3 as co-processor) Samsung Exynos 7420 (Cortex-M3 as a DVS microcontroller)[37] Texas Instruments F28, LM3, TMS470, OMAP 4470 (one Cortex-A9 + two Cortex-M3) XMOS XS1-XA (seven xCORE + one Cortex-M3) The following FPGAs include a Cortex-M3 core: Microsemi SmartFusion2 SoC The following vendors support the Cortex-M3 as soft-cores on their FPGA chips: Altera Cyclone-II, Cyclone-III, Stratix-II, Stratix-III Xilinx Spartan-3, Virtex-2, Virtex-3, Virtex-4, Artix-7[38] Cortex-M4Architecture and classificationMicroarchitectureARMv7E-MInstruction setThumb-1, Thumb-2,Saturated, DSP,Divide, FPU (SP) Silicon Labs (Energy Micro) Wonder Gecko STK Board with EFM32WG990 TI Stellaris Launchpad Board with LM4F120 Conceptually the Cortex-M4 is a Cortex-M3 plus DSP instructions, and optional floating-point unit (FPU). A core with an FPU is known as Cortex-M4F. Key features of the Cortex-M4 core are:[22] ARMv7E-M architecture[16] 3-stage pipeline with branch speculation. Instruction sets: Thumb-1 (entire). Thumb-2 (entire). 32-bit hardware integer multiply with 32-bit or 64-bit result, signed or unsigned, add or subtract after the multiply. 32-bit Multiply and MAC are 1 cycle. 32-bit hardware integer divide (2–12 cycles). Saturation arithmetic support. DSP extension: Single cycle 16/32-bit MAC, single cycle dual 16-bit MAC, 8/16-bit SIMD arithmetic. 1 to 240 interrupts, plus NMI. 12 cycle interrupt latency. Integrated sleep modes. Silicon options: Optional floating-point unit (FPU): single-precision only IEEE-754 compliant. It is called the FPv4-SP extension. Optional memory protection unit (MPU): 0 or 8 regions. nRF52833 on a micro bit v2 STM32F407IGH6 The following microcontrollers are based on the Cortex-M4 core: Analog Devices ADSP-CM40x Microchip (Atmel) SAM 4L, 4N, 4S NXP (Freescale) Kinetis K, W2 ST (STM32) WL (one Cortex-M4 + one Cortex-M0+) Texas Instruments SimpleLink Wi-Fi CC32xx, CC32xxMOD The following microcontrollers are based on the Cortex-M4F (M4 + FPU) core: Analog Devices ADUCM4050 Cypress 6200 (one Cortex-M4F + one Cortex-M0+), FM4 Infineon XMC4000 Maxim Darwin Microchip (Atmel) SAM4C (Dual core: one Cortex-M4F + one Cortex-M4), SAM4E, SAM4L, SAM4N, SAM4S, SAMG5, SAMD5/E5x Nordic nRF52 Nuvoton NuMicro M480 NXP LPC4000, LPC4300 (one Cortex-M4F + one Cortex-M0), LPC54000 NXP (Freescale) Kinetis K, V3, V4, S32K14x Renesas S3, S5, S7, RA4, RA6 Silicon Labs (Energy Micro) EFM32 Wonder ST STM32 F3, F4, L4, L4+, G4, WB (one Cortex-M4F + one Cortex-M0+) Texas Instruments LM4F, TM4C, MSP432, CC13x2R, CC1352P, CC26x2R Toshiba TX04 The following chips have either a Cortex-M4 or M4F as a secondary core: NXP (Freescale) Vybrid VF6 (one Cortex-A5 + one Cortex-M4F) NXP (Freescale) i.MX 6 SoloX (one Cortex-A9 + one Cortex-M4F) NXP (Freescale) i.MX 7 Solo/Dual (one or two Cortex-A7 + one Cortex-M4F) NXP (Freescale) i.MX 8 (two Cortex-A72 + four Cortex-A53 + two Cortex-M4F) NXP (Freescale) i.MX 8M and 8M Mini (four Cortex-A53 + one Cortex-M4F) NXP (Freescale) i.MX 8X (four Cortex-A35 + one Cortex-M4F) ST STM32MP1 (one or two Cortex-A7 + one Cortex-M4) Texas Instruments OMAP 5 (two Cortex-A15s + two Cortex-M4) Texas Instruments Sitara AM5700 (one or two Cortex-A15s + two Cortex-M4s as image processing units + two Cortex-M4s as general purpose units) Cortex-M7Architecture and classificationMicroarchitectureARMv7E-MInstruction setThumb-1, Thumb-2,Saturated, DSP,Divide, FPU (SP & DP) Arduino GIGA R1 WiFi board with (dual core ARM Cortex-M7 + ARM Cortex-M4) STM32H747XIH6 microcontroller The Cortex-M7 is a high-performance core with almost double the power efficiency of the older Cortex-M4.[7] It features a 6-stage superscalar pipeline with branch prediction and an optional floating-point unit capable of single-precision and optionally double-precision operations.[7][39] The instruction and data buses have been enlarged to 64-bit wide over the previous 32-bit buses. If a core contains an FPU, it is known as a Cortex-M7F, otherwise it is a Cortex-M7. Key features of the Cortex-M7 core are:[23] ARMv7E-M architecture. 6-stage pipeline with branch speculation. Second-longest of all ARM Cortex-M cores, with the first being Cortex-M85. Instruction sets: Thumb-1 (entire). Thumb-2 (entire). 32-bit hardware integer multiply with 32-bit or 64-bit result, signed or unsigned, add or subtract after the multiply. 32-bit Multiply and MAC are 1 cycle. 32-bit hardware integer divide (2–12 cycles). Saturation arithmetic support. DSP extension: Single cycle 16/32-bit MAC, single cycle dual 16-bit MAC, 8/16-bit SIMD arithmetic. 1 to 240 interrupts, plus NMI. 12 cycle interrupt latency. Integrated sleep modes. Silicon options: Optional floating-point unit (FPU): (single precision) or (single and double-precision), both IEEE-754-2008 compliant. It is called the FPv5 extension. Optional CPU cache: 0 to 64 KB instruction-cache, 0 to 64 KB data-cache, each with optional ECC. Optional Tightly-Coupled Memory (TCM): 0 to 16 MB instruction-TCM, 0 to 16 MB data-TCM, each with optional ECC. Optional Memory Protection Unit (MPU): 8 or 16 regions. Optional Embedded Trace Macrocell (ETM): instruction-only, or instruction and data. Optional Retention Mode (with Arm Power Management Kit) for Sleep Modes. Optional dual-redundant lock-step operation. The following microcontrollers are based on the Cortex-M7 core: Microchip (Atmel) SAM E7, S7, V7 NXP (Freescale) Kinetis KV5x, i.MX RT, S32K3xx ST STM32 F7, H7 Cortex-M23Architecture and classificationMicroarchitectureARMv8-M BaselineInstruction setThumb-1 (most),Thumb-2 (some),Divide, TrustZone The Cortex-M23 core was announced in October 2016[40] and based on the ARMv8-M architecture that was previously announced in November 2015.[41] Conceptually the Cortex-M23 is similar to a Cortex-M0+ plus integer divide instructions and TrustZone security features, and also has a 2-stage instruction pipeline.[8] Key features of the Cortex-M23 core are:[24][40] ARMv8-M Baseline architecture.[31] 2-stage pipeline. (similar to Cortex-M0+) TrustZone security instructions. 32-bit hardware integer divide (17 or 34 cycles).(slower than divide in all other cores) Stack limit boundaries. (available only with SAU option) Silicon options: Hardware integer multiply speed: 1 or 32 cycles. Hardware integer divide speed: 17 or 34 cycles maximum. Depending on divisor, instruction may complete in fewer cycles. Optional Memory Protection Unit (MPU): 0, 4, 8, 12, 16 regions. Optional Security Attribution Unit (SAU): 0, 4, 8 regions. Single-cycle I/O port (available in M0+/M23). Micro Trace Buffer (MTB) The following microcontrollers are based on the Cortex-M23 core: GigaDevice GD32E2xx Microchip SAM L10, L11, and PIC 32CM-LE 32CM-LS Nuvoton M23xx family, M2xx family, NUC1262, M2L31 Renesas S1JA, RA2A1, RA2L1, RA2E1, RA2E2 Cortex-M33Architecture and classificationMicroarchitectureARMv8-M MainlineInstruction setThumb-1, Thumb-2,Saturated, DSP,Divide, FPU (SP),TrustZone, Co-processor The Cortex-M33 core was announced in October 2016[40] and based on the ARMv8-M architecture that was previously announced in November 2015.[41] Conceptually the Cortex-M33 is similar to a cross of Cortex-M4 and Cortex-M23, and also has a 3-stage instruction pipeline.[9] Key features of the Cortex-M33 core are:[25][40] ARMv8-M Mainline architecture.[31] 3-stage pipeline. TrustZone security instructions. 32-bit hardware integer divide (11 cycles maximum). Stack limit boundaries. (available only with SAU option) Silicon options: Optional Floating-Point Unit (FPU): single-precision only IEEE-754 compliant. It is called the FPv5 extension. Optional Memory Protection Unit (MPU): 0, 4, 8, 12, 16 regions. Optional Security Attribution Unit (SAU): 0, 4, 8 regions. Micro Trace Buffer (MTB) The following microcontrollers are based on the Cortex-M33 core: Analog Devices ADUCM4 Dialog DA1469x GigaDevice GD32E5, GD32W5 Nordic nRF91, nRF5340, nRF54, nRF54H20[42] NXP LPC5500, i.MX RT600, MCX N94x/54x (dual core) ON RSL15 Renesas RA4, RA6 ST STM32 H5, L5, U5, WBA Silicon Labs Wireless Gecko Series 2 Texas Instruments CC3501E, CC3551E Raspberry Pi RP2350 The following chips have a Cortex-M33 or M33F as a secondary core: Infineon PSoC Edge ST STM32MP2 (one or two Cortex-A35 + one Cortex-M33) Cortex-M35PArchitecture and classificationMicroarchitectureARMv8-M MainlineInstruction setThumb-1, Thumb-2,Saturated, DSP,Divide, FPU (SP),TrustZone, Co-processor The Cortex-M35P core was announced in May 2018 and based on the Armv8-M architecture. It is conceptually a Cortex-M33 core with a new instruction cache, plus new tamper-resistant hardware concepts borrowed from the ARM SecurCore family, and configurable parity and ECC features.[10] Currently, information about the Cortex-M35P is limited, because its Technical Reference Manual and Generic User Guide haven't been released yet. The following microcontrollers are based on the Cortex-M35P core: STMicroelectronics ST33K Cortex-M52Architecture and classificationMicroarchitectureARMv8.1-M Mainline HeliumInstruction setThumb-1, Thumb-2,Saturated, DSP,Divide, FPU (VFPv5),TrustZone, Coprocessor, MVE The Cortex-M52 core was announced in November 2023 and based on the Armv8.1-M architecture. Conceptually, it can be seen as a cross between the Cortex-M33 and the Cortex-M55. Key differences are that its Helium co-processor is single beat (the M55 is dual beat), and it has a 32-bit main bus similar to the M33 to ease transition of applications. It has a 4 stage instruction pipeline.[11] Key features of the Cortex-M52 core include: ARMv8.1-M Mainline/Helium architecture.[31] 4-stage pipeline. Stack limit boundaries (available only with SAU option). 32-bit main bus (AHB or AXI)[11] Silicon options: Helium (M-Profile Vector Extension, MVE) Pointer Authentication and Branch Target Identification Extension Single-Precision and Double-Precision floating-point Digital Signal Processing (DSP) extension support TrustZone security extension support Safety and reliability (RAS) support Coprocessor support Secure and Non-secure MPU with 0, 4, 8, 12, or 16 regions SAU with 0, 4, or 8 regions Instruction cache with size of up to 64 KB Data cache with size of up to 64 KB ECC on caches and TCMs 1–480 interrupts 3–8 exception priority bits Internal and external WIC options, optional CTI, ITM, and DWT ARM Custom Instructions The following microcontrollers are based on the Cortex M52 core Geehy Semiconductor G32R5[43] Cortex-M55Architecture and classificationMicroarchitectureARMv8.1-M Mainline HeliumInstruction setThumb-1, Thumb-2,Saturated, DSP,Divide, FPU (VFPv5),TrustZone, Coprocessor, MVE The Cortex-M55 core was announced in February 2020 and based on the Armv8.1-M architecture. It has a 4 or 5 stage instruction pipeline.[12] Key features of the Cortex-M55 core include: ARMv8.1-M Mainline/Helium architecture.[31] 4-stage pipeline. Stack limit boundaries (available only with SAU option). 64-bit AXI main bus[12] Silicon options: Helium (M-Profile Vector Extension, MVE) Single-Precision and Double-Precision floating-point Digital Signal Processing (DSP) extension support TrustZone security extension support Safety and reliability (RAS) support Coprocessor support Secure and Non-secure MPU with 0, 4, 8, 12, or 16 regions SAU with 0, 4, or 8 regions Instruction cache with size of 4 KB, 8 KB, 16 KB, 32 KB, 64 KB Data cache with size of 4 KB, 8 KB, 16 KB, 32 KB, 64 KB ECC on caches and TCMs 1–480 interrupts 3–8 exception priority bits Internal and external WIC options, optional CTI, ITM, and DWT ARM Custom Instructions Alif Semiconductor Ensemble & Balletto MCU families offer single or dual Cortex-M55 cores, each paired with Ethos-U55 NPUs Infineon PSoC Edge ST STM32 N6 Cortex-M85Architecture and classificationMicroarchitectureARMv8.1-M Mainline HeliumInstruction setThumb-1, Thumb-2,Saturated, DSP,Divide, FPU (VFPv5),TrustZone, Coprocessor, MVE The Cortex-M85 core was announced in April 2022 and based on the Armv8.1-M architecture. It has a 7-stage instruction pipeline.[13] Silicon options: Optional CPU cache: 0 to 64 KB instruction-cache, 0 to 64 KB data-cache, each with optional ECC. Optional Tightly-Coupled Memory (TCM): 0 to 16 MB instruction-TCM, 0 to 16 MB data-TCM, each with optional ECC. Optional Memory Protection Unit (MPU): 16 regions. Can have separate ones for secure and non-secure mode if TrustZone is implemented. Up to 480 interrupts and NMI 3–8 exception priority bits Optional dual-redundant lock-step operation. Renesas RA8 Main article: List of ARM Cortex-M development tools The documentation for ARM chips is extensive. In the past, 8-bit microcontroller documentation would typically fit in a single document, but as microcontrollers have evolved, so has everything required to support them. A documentation package for ARM chips typically consists of a collection of documents from the IC manufacturer as well as the CPU core vendor (ARM Limited). A typical top-down documentation tree is: Documentation tree (top to bottom) IC manufacturer website. IC manufacturer marketing slides. IC manufacturer datasheet for the exact physical chip. IC manufacturer reference manual that describes common peripherals and aspects of a physical chip family. ARM core website. ARM core generic user guide. ARM core technical reference manual. ARM architecture reference manual. IC manufacturers have additional documents, such as: evaluation board user manuals, application notes, getting started guides, software library documents, errata, and more. See External links section for links to official Arm documents. Electronics portal ARM architecture List of ARM architectures and cores Interrupt, Interrupt handler Real-time operating system, Comparison of real-time operating systems

^ ARM Cortex-M website; ARM Limited. ^ a b "Cortex-M0 Home". ARM Limited. ^ "Cortex-M0+ Home". ARM Limited. ^ a b "Cortex-M1 Home". ARM Limited. ^ "Cortex-M3 Home". ARM Limited. ^ "Cortex-M4 Home". ARM Limited. ^ a b c "Cortex-M7 Home". ARM Limited. ^ a b "Cortex-M23 Home". ARM Limited. ^ a b "Cortex-M33 Home". ARM Limited. ^ a b c "Cortex-M35P Home". ARM Limited. ^ a b c "Cortex-M52 Home". ARM Limited. ^ a b c "Cortex-M55 Home". ARM Limited. ^ a b "Cortex-M85 Home". ARM Limited. ^ "On Hacking MicroSD Cards". ^ a b c d e f g h i j k l m n o p q r "ARMv6-M Architecture Reference Manual". ARM Limited. ^ a b c d e f g h i j k l m n o p q r "ARMv7-M Architecture Reference Manual". ARM Limited. ^ a b c d Cortex-M3 Embedded Software Development; App Note 179; ARM Limited. ^ a b c "Cortex-M0 Technical Reference Manual". ARM Limited. ^ a b c d "Cortex-M0+ Technical Reference Manual". ARM Limited. ^ a b c "Cortex-M1 Technical Reference Manual". ARM Limited. ^ a b c "Cortex-M3 Technical Reference Manual". ARM Limited. ^ a b c "Cortex-M4 Technical Reference Manual". ARM Limited. ^ a b c d "Cortex-M7 Technical Reference Manual". ARM Limited. ^ a b c "Cortex-M23 Technical Reference Manual". ARM Limited. ^ a b c "Cortex-M33 Technical Reference Manual". ARM Limited. ^ a b "Cortex-M52 Technical Reference Manual". ARM Limited. ^ a b "Cortex-M55 Technical Reference Manual". ARM Limited. ^ a b "Cortex-M85 Technical Reference Manual". ARM Limited. ^ a b c "Cortex-M System Design Kit (CMSDK)". Arm Holdings. Archived from the original on March 4, 2016. ^ a b c d e f g h i j ARM Cortex-M Programming Guide to Memory Barrier Instructions; Section 3.6 System implementation requirements; AppNote 321; ARM Limited. ^ a b c d e f g h i j k l "ARMv8-M Architecture Reference Manual". ARM Limited. ^ 32-bit PIC and SAM Microcontrollers; Microchip. ^ Fingas, Jon (25 February 2014). "Freescale makes the world's smallest ARM controller chip even tinier". Retrieved 2 October 2014. ^ GOWIN Semiconductor joins ARM DesignStart offering free ARM Cortex-M1 Processors for its FPGA product families ^ Cortex-M1 DesignStart FPGA XilinxEdition; ARM Limited. ^ Sadasivan, Shyam. "An Introduction to the ARM Cortex-M3 Processor" (PDF). ARM Limited. Archived from the original (PDF) on July 26, 2014. ^ "Samsung Exynos 7420 Deep Dive - Inside a Modern 14nm SoC". AnandTech. Retrieved 2015-06-15. ^ Cortex-M3 DesignStart FPGA XilinxEdition ^ "ARM Supercharges MCU Market with High Performance Cortex-M7 Processor". ARM Limited (Press release). September 24, 2014. ^ a b c d New ARM Cortex-M processors offer the next industry standard for secure IoT; ARM Limited; October 25, 2016. ^ a b ARMv8-M Architecture Simplifies Security for Smart Embedded Devices; ARM Limited; November 10, 2015. ^ "nRF54H20 - Nordic Semiconductor". www.nordicsemi.com. Retrieved 2024-10-30. ^ "The World's First Dual-Core Real-Time Control MCU Featuring Cortex-M52 Processor Unveiled at Electronica China 2024". Designer's Guide to the Cortex-M Processor Family; 3rd Ed; Trevor Martin; 648 pages; 2022; ISBN 978-0323854948. Definitive Guide to the ARM Cortex-M0 and Cortex-M0+ Processors; 2nd Ed; Joseph Yiu; 784 pages; 2015; ISBN 978-0128032770. Definitive Guide to the ARM Cortex-M3 and Cortex-M4 Processors; 3rd Ed; Joseph Yiu; 864 pages; 2013; ISBN 978-0124080829. Definitive Guide to the ARM Cortex-M23 and Cortex-M33 Processors; 1st Ed; Joseph Yiu; 928 pages; 2020; ISBN 978-0128207352. Microcontrollers with C: Cortex-M and Beyond; 1st Ed; Klaus Elk; 227 pages; 2023; ISBN 979-8862003437. Embedded Systems with ARM Cortex-M Microcontrollers in Assembly Language and C; 4th Ed; Yifeng Zhu; 730 pages; 2023; ISBN 978-0982692677. ARM Assembly for Embedded Applications; 5th Ed; Daniel Lewis; 379 pages; 2019; ISBN 978-1092542234. Assembly Language Programming: ARM Cortex-M3; 1st Ed; Vincent Mahout; 256 pages; 2012; ISBN 978-1848213296. Digital Signal Processing and Applications Using the ARM Cortex-M4; 1st Ed; Donald Reay; 320 pages; 2015; ISBN 978-1118859049. Hands-On RTOS with Microcontrollers; 1st Ed; Brian Amos; 496 pages; 2020; ISBN 978-1838826734. Wikimedia Commons has media related to ARM Cortex-M. ARM Cortex-M official documents ARM Cortex-M official website Cortex-M for Beginners arm.com ARMv8-M Security Extensions arm.com Cortex Microcontroller Software Interface Standard (CMSIS) arm.com ARMcore Bitwidth ARMwebsite ARM genericuser guide ARM technicalreference manual ARM architecturereference manual Cortex-M0 32 Link Link Link ARMv6-M Cortex-M0+ 32 Link Link Link ARMv6-M Cortex-M1 32 Link Link Link ARMv6-M Cortex-M3 32 Link Link Link ARMv7-M Cortex-M4 32 Link Link Link ARMv7E-M Cortex-M7 32 Link Link Link ARMv7E-M Cortex-M23 32 Link Link Link ARMv8-M Cortex-M33 32 Link Link Link ARMv8-M Cortex-M35P 32 Link N/A N/A ARMv8-M Cortex-M52 32 Link Link Link ARMv8.1-M Cortex-M55 32 Link Link Link ARMv8.1-M Cortex-M85 32 Link Link Link ARMv8.1-M Quick reference cards Instructions: Thumb-1 (1), ARM and Thumb-2 (2), Vector Floating-Point (3) arm.com Opcodes: Thumb-1 (1, 2), ARM (3, 4), GNU Assembler Directives (5). Migrating Migrating from 8051 to Cortex-M3 – arm.com Migrating from PIC to Cortex-M3 – arm.com Migrating from ARM7TDMI to Cortex-M3 – arm.com Migrating from Cortex-M4 to Cortex-M7 – keil.com Other Bit Banding on STM32 Cortex-M microcontrollers Retrieved from " Italian open-source hardware and software company "LilyPad" redirects here. For other uses, see Lily pad (disambiguation). For other uses, see Arduino (disambiguation). ArduinoArduino Uno SMD R3ManufacturerArduinoTypeSingle-board microcontrollerOperating systemNone, with bootloader (default) Xinu FreeRTOSCPU Atmel AVR (8-bit) ARM Cortex-M0+ (32-bit) ARM Cortex-M3 (32-bit) Intel Quark (x86) (32-bit) MemorySRAMStorageFlash, EEPROMWebsitearduino.cc Arduino (/ɑːrˈdwiːnoʊ/) is an Italian open-source hardware and software company, project, and user community that designs and manufactures single-board microcontrollers and microcontroller kits for building digital devices. Its hardware products are licensed under a CC BY-SA license, while the software is licensed under the GNU Lesser General Public License (LGPL) or the GNU General Public License (GPL),[1] permitting the manufacture of Arduino boards and software distribution by anyone. Arduino boards are available commercially from the official website or through authorized distributors.[2] Arduino board designs use a variety of microprocessors and controllers. The boards are equipped with sets of digital and analog input/output (I/O) pins that may be interfaced to various expansion boards ('shields') or breadboards (for prototyping) and other circuits. The boards feature serial communications interfaces, including Universal Serial Bus (USB) on some models, which are also used for loading programs. The microcontrollers can be programmed using the C and C++ programming languages (Embedded C), using a standard API which is also known as the Arduino Programming Language, inspired by the Processing language and used with a modified version of the Processing IDE. In addition to using traditional compiler toolchains, the Arduino project provides an integrated development environment (IDE) and a command line tool developed in Go. The Arduino project began in 2005 as a tool for students at the Interaction Design Institute Ivrea, Italy,[3] aiming to provide a low-cost and easy way for novices and professionals to create devices that interact with their environment using sensors and actuators. Common examples of such devices intended for beginner hobbyists include simple robots, thermostats, and motion detectors. The name Arduino comes from a café in Ivrea, Italy, where some of the project's founders used to meet. The bar was named after Arduin of Ivrea, who was the margrave of the March of Ivrea and King of Italy from 1002 to 1014.[4] The first prototype[3] The Arduino project was started at the Interaction Design Institute Ivrea (IDII) in Ivrea, Italy.[3] At that time, the students used a BASIC Stamp microcontroller at a cost of $50. In 2004, Hernando Barragán created the development platform Wiring as a Master's thesis project at IDII, under the supervision of Massimo Banzi and Casey Reas. Casey Reas is known for co-creating, with Ben Fry, the Processing development platform. The project goal was to create simple, low cost tools for creating digital projects by non-engineers. The Wiring platform consisted of a printed circuit board (PCB) with an ATmega128 microcontroller, an IDE based on Processing and library functions to easily program the microcontroller.[5] In 2005, Massimo Banzi, with David Mellis, another IDII student, and David Cuartielles, extended Wiring by adding support for the cheaper ATmega8 microcontroller. The new project, forked from Wiring, was called Arduino.[5] The initial Arduino core team consisted of Massimo Banzi, David Cuartielles, Tom Igoe, Gianluca Martino, and David Mellis.[3] Following the completion of the platform, lighter and less expensive versions were distributed in the open-source community. It was estimated in mid-2011 that over 300,000 official Arduinos had been commercially produced,[6] and in 2013 that 700,000 official boards were in users' hands.[7] In early 2008, the five co-founders of the Arduino project created a company, Arduino LLC,[8] to hold the trademarks associated with Arduino. The manufacture and sale of the boards were to be done by external companies, and Arduino LLC would get a royalty from them. The founding bylaws of Arduino LLC specified that each of the five founders transfer ownership of the Arduino brand to the newly formed company.[citation needed] At the end of 2008, Gianluca Martino's company, Smart Projects, registered the Arduino trademark in Italy and kept this a secret from the other co-founders for about two years. This was revealed when the Arduino company tried to register the trademark in other areas of the world (they originally registered only in the US), and discovered that it was already registered in Italy. Negotiations with Martino and his firm to bring the trademark under the control of the original Arduino company failed. In 2014, Smart Projects began refusing to pay royalties. They then appointed a new CEO, Federico Musto, who renamed the company Arduino SRL and created the website arduino.org, copying the graphics and layout of the original arduino.cc. This resulted in a rift in the Arduino development team.[9][10][11] In January 2015, Arduino LLC filed a lawsuit against Arduino SRL.[12] In May 2015, Arduino LLC created the worldwide trademark Genuino, used as brand name outside the United States.[13] At the World Maker Faire in New York on 1 October 2016, Arduino LLC co-founder and CEO Massimo Banzi and Arduino SRL CEO Federico Musto announced the merger of the two companies, forming Arduino AG.[14] Around that same time, Massimo Banzi announced that in addition to the company a new Arduino Foundation would be launched as "a new beginning for Arduino", but this decision was withdrawn later.[15][16][17] In April 2017, Wired reported that Musto had "fabricated his academic record.... On his company's website, personal LinkedIn accounts, and even on Italian business documents, Musto was, until recently, listed as holding a Ph.D. from the Massachusetts Institute of Technology. In some cases, his biography also claimed an MBA from New York University." Wired reported that neither university had any record of Musto's attendance, and Musto later admitted in an interview with Wired that he had never earned those degrees.[18] The controversy surrounding Musto continued when, in July 2017, he reportedly pulled many open source licenses, schematics, and code from the Arduino website, prompting scrutiny and outcry.[19] By 2017 Arduino 'AG' owned many Arduino trademarks. In July 2017 BCMI, founded by Massimo Banzi, David Cuartielles, David Mellis and Tom Igoe, acquired Arduino AG and all the Arduino trademarks. Fabio Violante is the new CEO replacing Federico Musto, who no longer works for Arduino AG.[20][21] In October 2017, Arduino announced its partnership with Arm Holdings (ARM). The announcement said, in part, "ARM recognized independence as a core value of Arduino ... without any lock-in with the ARM architecture". Arduino intends to continue to work with all technology vendors and architectures.[22] Under Violante's guidance, the company started growing again and releasing new designs. The Genuino trademark was dismissed and all products were branded again with the Arduino name. In August 2018, Arduino announced its new open source command line tool (arduino-cli), which can be used as a replacement of the IDE to program the boards from a shell.[23] In February 2019, Arduino announced its IoT Cloud service as an extension of the Create online environment.[24] As of February 2020, the Arduino community included about 30 million active users based on the IDE downloads.[25] Arduino-compatible R3 Uno board with no Arduino logo Arduino is open-source hardware. The hardware reference designs are distributed under a Creative Commons Attribution Share-Alike 2.5 license and are available on the Arduino website. Layout and production files for some versions of the hardware are also available. Although the hardware and software designs are freely available under copyleft licenses, the developers have requested the name Arduino to be exclusive to the official product and not be used for derived works without permission. The official policy document on the use of the Arduino name emphasizes that the project is open to incorporating work by others into the official product.[26] Several Arduino-compatible products commercially released have avoided the project name by using various names ending in -duino.[27] An early Arduino board[28] with an RS-232 serial interface (upper left) and an Atmel ATmega8 microcontroller chip (black, lower right); the 14 digital I/O pins are at the top, the 6 analog input pins at the lower right, and the power connector at the lower left. Most Arduino boards consist of an Atmel 8-bit AVR microcontroller (ATmega8,[29] ATmega168, ATmega328, ATmega1280, or ATmega2560) with varying amounts of flash memory, pins, and features.[30] The 32-bit Arduino Due, based on the Atmel SAM3X8E was introduced in 2012.[31] The boards use single or double-row pins or female headers that facilitate connections for programming and incorporation into other circuits. These may connect with add-on modules termed shields. Multiple and possibly stacked shields may be individually addressable via an I^2C serial bus. Most boards include a 5 V linear regulator and a 16 MHz crystal oscillator or ceramic resonator. Some designs, such as the LilyPad,[32] run at 8 MHz and dispense with the onboard voltage regulator due to specific form factor restrictions. Arduino microcontrollers are pre-programmed with a bootloader that simplifies the uploading of programs to the on-chip flash memory. The default bootloader of the Arduino Uno is the Optiboot bootloader.[33] Boards are loaded with program code via a serial connection to another computer. Some serial Arduino boards contain a level shifter circuit to convert between RS-232 logic levels and transistor–transistor logic (TTL serial) level signals. Current Arduino boards are programmed via Universal Serial Bus (USB), implemented using USB-to-serial adapter chips such as the FTDI FT232. Some boards, such as later-model Uno boards, substitute the FTDI chip with a separate AVR chip containing USB-to-serial firmware, which is reprogrammable via its own ICSP header. Other variants, such as the Arduino Mini and the unofficial Boarduino, use a detachable USB-to-serial adapter board or cable, Bluetooth or other methods. When used with traditional microcontroller tools, instead of the Arduino IDE, standard AVR in-system programming (ISP) programming is used. An official Arduino Uno R2 with descriptions of the I/O locations The Arduino board exposes most of the microcontroller's I/O pins for use by other circuits. The Diecimila,[a] Duemilanove,[b] and current Uno[c] provide 14 digital I/O pins, six of which can produce pulse-width modulated signals, and six analog inputs, which can also be used as six digital I/O pins. These pins are on the top of the board, via female 0.1-inch (2.54 mm) headers. Several plug-in application shields are also commercially available. The Arduino Nano and Arduino-compatible Bare Bones Board[34] and Boarduino[35] boards may provide male header pins on the underside of the board that can plug into solderless breadboards. Many Arduino-compatible and Arduino-derived boards exist. Some are functionally equivalent to an Arduino and can be used interchangeably. Many enhance the basic Arduino by adding output drivers, often for use in school-level education,[36] to simplify making buggies and small robots. Others are electrically equivalent, but change the form factor, sometimes retaining compatibility with shields, sometimes not. Some variants use different processors, of varying compatibility. In addition to hardware variations, open source libraries have been developed to support Arduino hardware in EDA tools. One such project provides KiCad schematic symbols and PCB footprints for Arduino modules, expansion boards, and connectors, making it easier for engineers to integrate Arduino into their designs. [37] Further information: List of Arduino boards and compatible systems The original Arduino hardware was manufactured by the Italian company Smart Projects.[38] Some Arduino-branded boards have been designed by the American companies SparkFun Electronics and Adafruit Industries.[39] As of 2016[update], 17 versions of the Arduino hardware have been commercially produced. Arduino RS232[40](male pins) Arduino Diecimila[41] Arduino Duemilanove[42](rev 2009b) Arduino Uno R2[43][44] Arduino Uno SMD R3[45] Arduino Leonardo[46] Arduino Micro (ATmega32U4) Arduino Pro Micro (ATmega32U4) Arduino Pro[47](No USB) Arduino Mega[48] Arduino Nano[49](DIP-30 footprint) Arduino LilyPad 00[50](rev 2007) (No USB) Arduino Robot[51] Arduino Esplora[52] Arduino Ethernet[53](AVR + W5100) Arduino Yún[54](AVR + AR9331) Arduino Due[55](ARM Cortex-M3 core) Arduino GIGA R1 WiFi (Dual core ARM Cortex-M7 + ARM Cortex-M4 cores + Murata 1DX) Arduino and Arduino-compatible boards use printed circuit expansion boards called shields, which plug into the normally supplied Arduino pin headers.[56] Shields can provide motor controls for 3D printing and other applications, GNSS (satellite navigation), Ethernet, liquid crystal display (LCD), or breadboarding (prototyping). Several shields can also be made do it yourself (DIY).[57][58][59] Some shields offer stacking headers which allow multiple shields to be stacked on top of an Arduino board. Here, a prototyping shield is stacked on two Adafruit motor shield V2s. Screw-terminal breakout shield in a wing-type format, allowing bare-end wires to be connected to the board without requiring any specialized pins Adafruit Datalogging Shield with a Secure Digital (SD) card slot and real-time clock (RTC) chip along with some space for adding components and modules for customization Adafruit Motor Shield with screw terminals for connection to motors. Officially discontinued, this shield may still be available through unofficial channels. The

Adafruit Motor Shield V2 uses I2C, requiring vastly fewer digital I/O pins than attaching each motor directly. A USB host shield which allows an Arduino board to communicate with a USB device such as a keyboard or a mouse A program for Arduino hardware may be written in any programming language with compilers that produce binary machine code for the target processor. Atmel provides a development environment for their 8-bit AVR and 32-bit ARM Cortex-M based microcontrollers: AVR Studio (older) and Atmel Studio (newer).[60][61][62] Arduino Legacy IDEScreenshot of Arduino Legacy IDE showing Blink programDeveloper(s)Arduino SoftwareStable release1.8.19 / 21 December 2021; 3 years ago (2021-12-21)[63] Written inJava, C, C++Operating systemMicrosoft Windows, macOS, LinuxPlatformIA-32, x86-64, ARMTypeIntegrated development environmentLicenseLGPL or GPL licenseWebsitewww.arduino.cc/en/software The Arduino integrated development environment (IDE) is a cross-platform application (for Microsoft Windows, macOS, and Linux) that is based on Processing IDE which is written in Java. It uses the Wiring API as programming style and HAL. It includes a code editor with features such as text cutting and pasting, searching and replacing text, automatic indenting, brace matching, and syntax highlighting, and provides simple one-click mechanisms to compile and upload programs to an Arduino board. It also contains a message area, a text console, a toolbar with buttons for common functions and a hierarchy of operation menus. The source code for the IDE is released under the GNU General Public License, version 2.[64] The Arduino IDE supports the languages C and C++ using special rules of code structuring. The Arduino IDE supplies a software library from the Wiring project, which provides many common input and output procedures. User-written code only requires two basic functions, for starting the sketch and the main program loop, that are compiled and linked with a program stub main() into an executable cyclic executive program with the GNU toolchain, also included with the IDE distribution. The Arduino IDE employs the program avrdude to convert the executable code into a text file in hexadecimal encoding that is loaded into the Arduino board by a loader program in the board's firmware. Traditionally, Arduino IDE was used to program Arduino's official boards based on Atmel AVR Microcontrollers, but over time, once the popularity of Arduino grew and the availability of open-source compilers existed, many more platforms from PIC, STM32, TI MSP430, ESP32 can be coded using Arduino IDE.[65] Arduino IDEScreenshot of Arduino IDE 2.x showing Blink codeDeveloper(s)Arduino SoftwareStable release2.3.2 / 20 February 2024; 16 months ago (2024-02-20)[66] Written inTypeScript, JavaScript, GoOperating systemMicrosoft Windows, macOS, LinuxPlatformx86-64TypeIntegrated development environmentLicenseGNU Affero General Public License v3.0Websitewww.arduino.cc/en/software An initial alpha preview of a new Arduino IDE was released on October 18, 2019, as Arduino Pro IDE. The beta preview was released on March 1, 2021, renamed IDE 2.0. On September 14, 2022, the Arduino IDE 2.0 was officially released as stable.[67] The system still uses Arduino CLI (Command Line Interface), but improvements include a more professional development environment and autocompletion support.[68] The application frontend is based on the Eclipse Theia Open Source IDE. Its main new features are:[69] Modern, fully featured development environment New Board Manager New Library Manager Project Explorer Basic Auto-Completion and syntax check Serial Monitor with Graph Plotter Dark Mode and DPI awareness 64-bit release Debugging capability One important feature Arduino IDE 2.0 provides is the debugging feature.[70] It allows users to single-step, insert breakpoints or view memory. Debugging requires a target chip with debug port and a debug probe. The official Arduino Zero board can be debugged out of the box. Other official Arduino SAMD21 boards require a separate SEGGER J-Link or Atmel-ICE. For a 3rd party board, debugging in Arduino IDE 2.0 is also possible as long as such board supports GDB, OPENOCD and has a debug probe. Community has contributed debugging for ATMega328P based Arduino [71] or CH32 RISC-V boards,[72] etc. A sketch is a program written with the Arduino IDE.[73] Sketches are saved on the development computer as text files with the file extension .ino. Arduino Software (IDE) pre-1.0 saved sketches with the extension .pde. A minimal Arduino C/C++ program consists of only two functions:[74] setup(): This function is called once when a sketch starts after power-up or reset. It is used to initialize variables, input and output pin modes, and other libraries needed in the sketch. It is analogous to the function main().[75] loop(): After setup() function exits (ends), the loop() function is executed repeatedly in the main program. It controls the board until the board is powered off or is reset. It is analogous to the function while(1).[76] Blink example Power LED (red) and User LED (green) attached to pin 13 on an Arduino-compatible board Most Arduino boards contain a light-emitting diode (LED) and a current-limiting resistor connected between pin 13 and ground, which is a convenient feature for many tests and program functions.[77] A typical program used by beginners, akin to Hello, World!, is "blink", which repeatedly blinks the on-board LED integrated into the Arduino board. This program uses the functions pinMode(), digitalWrite(), and delay(), which are provided by the internal libraries included in the IDE environment.[78][79][80] This program is usually loaded into a new Arduino board by the manufacturer. const int LED_PIN = 13; // Pin number attached to LED. void setup() { pinMode(LED_PIN, OUTPUT); // Configure pin 13 to be a digital output. } void loop() { digitalWrite(LED_PIN, HIGH); // Turn on the LED. delay(1000); // Wait 1 second (1000 milliseconds). digitalWrite(LED_PIN, LOW); // Turn off the LED. delay(1000); // Wait 1 second. } Sweep example Sweeping a servo with an Arduino means moving it back and forth across a specified range of motion. This is commonly done using the Servo library in Arduino. To sweep a servo with an Arduino, connect the servo's VCC (red wire) to 5V, GND (black/brown) to GND, and signal (yellow/white) to a PWM-capable pin (e.g., Pin 9). Use the Servo library to control movement. The code below gradually moves the servo from 0° to 180° and back in a loop.#include Servo myServo; // Create a Servo object void setup() { myServo.attach(9); // Attach servo to pin 9 } void loop() { for (int pos = 0; pos = 0; pos--) { // Move back from 180° to 0° myServo.write(pos); delay(15); } } The open-source nature of the Arduino project has facilitated the publication of many free software libraries that other developers use to augment their projects. There is a Xinu OS port for the ATmega328P (Arduino Uno and others with the same chip), which includes most of the basic features.[81] The source code of this version is freely available.[82] There is also a threading tool, named Protothreads. Protothreads are described as "extremely lightweight stackless threads designed for severely memory constrained systems, such as small embedded systems or wireless sensor network nodes.[83] There is a port of FreeRTOS for the Arduino.[84] This is available from the Arduino Library Manager. It is compatible with a number of boards, including the Uno. Arduboy, a handheld game console based on Arduino Arduinome, a MIDI controller device that mimics the Monome Ardupilot, drone software and hardware ArduSat, a cubesat based on Arduino C-STEM Studio, a platform for hands-on integrated learning of computing, science, technology, engineering, and mathematics (C-STEM) with robotics Data loggers for scientific research[85][86][87][88] OBDuino, a trip computer that uses the on-board diagnostics interface found in most modern cars OpenEVSE an open-source electric vehicle charger XOD, a visual programming language for Arduino Tinkercad Circuits - an analog and digital simulator supporting Arduino Simulation, which is commonly used to create 3D models The Arduino project received an honorary mention in the Digital Communities category at the 2006 Prix Ars Electronica.[89] The Arduino Engineering Kit won the Bett Award for "Higher Education or Further Education Digital Services" in 2020.[90] Free and open-source software portalElectronics portal List of Arduino boards and compatible systems List of open-source hardware projects Calliope mini BBC micro:bit Raspberry Pi ^ Diecimila means "ten thousand" in Italian ^ Duemilanove means "two thousand and nine" in Italian ^ Uno means "one" in Italian ^ "Getting Started: FOUNDATION > Introduction". arduino.cc. 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Official website How Arduino is open sourcing imagination, a TED talk by creator Massimo Banzi Evolution tree for Arduino Arduino Cheat Sheet Arduino Dimensions and Hole Patterns Arduino Shield Template Arduino Board Pinout Diagrams: Due, Esplora, Leonardo, Mega, Micro, Mini, Pro Micro, Pro Mini, Uno, Yun Historical Arduino – The Documentary (2010): IMDb, Vimeo Massimo Banzi interviews: Triangulation 110, FLOSS 61 Untold History of Arduino – Hernando Barragán Lawsuit documents from Arduino LLC vs. Arduino S.R.L. et al. – United States Courts Archive Retrieved from " 2Microcontroller family 78K Family microcontrollersGeneral informationLaunched1986; 39 years ago (1986)DiscontinuedcurrentCommon manufacturerRenesas Electronics(formerly NEC)PerformanceMax. CPU clock rate32 kHz to 24 MHzData width16/8Address width20(24)/16Architecture and classificationApplicationEmbeddedInstruction set78K FamilyPhysical specificationsCores1Products, models, variantsVariant78K0R, 78K0S, 78K0,78K4, 78K6, 78K3,78K7,78K1, 78K2HistoryPredecessors87AD Family,17K FamilySuccessorRL78 Family 78K0/KX1+ board with in-circuit emulator; MINICUBE 78K0S/KA1+ Do It board 78K0R/KG3 Cool It board with in-circuit emulator; IECUBE (formerly, MINICUBE2) 78K is the trademark name of 16- and 8-bit microcontroller family[1]:23-4–23-5[2]:78 manufactured by Renesas Electronics, originally developed by NEC[3][4]:229 started in 1986.[5]:7,line 2 The basis of 78K Family is an accumulator-based register-bank CISC architecture. 78K is a single-chip microcontroller, which usually integrates; program ROM, data RAM, serial interfaces, timers, I/O ports, an A/D converter, an interrupt controller, and a CPU core, on one die.[6][7]:412 Its application area is mainly simple mechanical system controls and man-machine interfaces.[8][9][10] Regarding software development tools, C compilers and macro-assemblers are available.[11]:99 As for development tool hardware, full probing-pod type and debug port type in-circuit emulators,[12][13] and flash ROM programmers[14]:22–24 are available. Historically, the family has 11 series with 9 instruction set architectures. As of 2018, 3 instruction set architectures, those are 8-bit 78K0, 8-bit 78K0S, and 16-/8-bit 78K0R, are still promoted for customers' new designs.[14] But in most of cases, migration to RL78 Family,[15] which is a successor of 78K0R and almost binary level compatible with 78K0R,[16]:20 is recommended.[17] 78K0 Series [de; jp] (also known as 78K/0) is a long-running 8-bit single chip microcontroller,[18] which is the basis of 78K0S [jp] and 78K0R Series. It contains 8× 8-bit registers ×4 banks. For 16-bit calculating instructions, it performs ALU operation twice. Each instructions are performed serially without instruction pipelining. It has 16-bit 64K Byte address space.[19] Some variants of 78K0 have affordable and compact type 8-bit R-2R D/A converter, which does not have monotonicity because it is not trimmed for adjustment nor followed by operational amplifier. In its earlier stage, the Program Memory was one-time PROM (OTP), UV-EPROM, or mask ROM.[20] But with the times, it became flash memory.[21][22] 78K0S Series (also known as 78K/0S) is a low-end version of 78K0.[23][24][25] It has 8× 8-bit registers, but without any banks. In addition, some instructions, such as multiplication and division, are removed from 78K0 instruction set architecture.[26] 78K0R Series is a 16-bit single-chip microcontroller with 3-stage instruction pipelining.[27] Its instruction set is similar to 78K0 and covers 16- and 8-bit operations. It has 20-bit 1M Byte address space.[28] 75 instructions out of 80 are identical with that of RL78 Family; its successor.[16]:20[15][29] 178K0 Series (also known as 178K/0) is a successor of NEC's 17K Family 4-bit microcontroller for DTS (Digital Tuning Systems) and remote controls.[30] It integrates 17K family's peripheral functions with the 78K0 8-bit CPU core on a chip.[31] 178K0S Series (also known as 178K/0S) is also successor of 17K Family with the 78K0S CPU core.[32] 78K4 Series (also known as 78K/4) is a 16-bit single-chip microcontroller with 16 and 8-bit operations.[33][34][35][36] It has 16× 8-bit registers ×4 banks, which can be also used for 8× 16-bit registers ×4 banks. Some of these registers can be also used as 24-bit extension for addressing modes.[37] It has 24-bit 16M Byte address space. It has microcode-based operations named Macro Service with interrupt functions.[38]:§23.8,560–593 78K7 Series (also known as 78K/7) is a 32-bit single-chip microcontroller with 32, 16 and 8 bit operations. It has 8× 32-bit registers ×16 banks, which can be also used for 16× 16-bit registers ×16 banks and 16× 8-bit registers ×16 banks. It has microcode-based operations named Macro Service with interrupt functions. It has 24-bit 16M Byte linear address space. It is used for some Quantum Fireball products,[39]:Photo 2 but shortly replaced with V850 Family 32-bit RISC microcontrollers. 78K6 Series (also known as 78K/6) is a 16-bit single-chip microcontroller. Its life-time was short, and less variants. 78K1 Series (also known as 78K/1) is an 8-bit single-chip microcontroller. It has 8× 8-bit registers ×4 banks. 78K1 series is targeted for servo controls of videocassette recorders. µPD78148 sub-series integrates 2 operational amplifiers.[40] 78K3 Series (also known as 78K/3) is a 16-bit single-chip microcontroller with 16 and 8 bit operations. It has 16× 8-bit ×8 banks, which can be also used for 8× 16-bit registers ×8 banks. Its address space is 16-bit 64K Byte. It is developed as high-end series of 78K Family. It has microcode-based operations named Macro Service with interrupt functions.[41]:§13.4,261–280 This series is used for hard disk drives, especially Quantum Fireball Series.[42] µPD78364 sub-series is used for inverter compressor controls.[43] It is also used for traction control systems of some cars. 78K2 Series (also known as 78K/2) is an 8-bit single-chip microcontroller. It has 8× 8-bit registers ×4 banks. It is developed as general purpose series of 78K Family.[44] 87AD Family[4]:229 is an 8-bit single-chip microcontroller. It has 8× 8-bit registers ×4 banks. Its instruction set architecture became the basis of 78K.[45] 17K Family[4]:229 is a 4-bit single-chip microcontroller, especially dedicated for DTS (Digital Tuning Systems) and remote controls. It has 2 plane of 128× 4-bit register files, and sophisticated fully orthogonal instruction set. This instruction set is completely different from that of 78K Family.[30] Series ALU Registers Instructions Pipeline Remark Documents RL78-S3 16-bit 8× 8-bit ×4 banks 81 (75+6) 3-stage Successor of 78K0R [29]:8 RL78-S2 16-bit 8× 8-bit ×4 banks 75 3-stage RL78-S1 8-bit 8× 8-bit (no bank) 74 (75-1) 3-stage 78K0R 16-bit 8× 8-bit ×4 banks 80 (75+5) 3-stage Extended 78K0/ [28]:18 78K0S 8-bit 8× 8-bit (no bank) 47 none Simplified 78K0/ [25] 78K0 8-bit 8× 8-bit ×4 banks 48 none Basic 78K/0 core [19] 178K0S 8-bit 8× 8-bit 47 none 78K/0S for DTS;Digital Tuning System [25][32] 178K0 8-bit 8× 8-bit ×4 banks 48 none 78K/0 for DTS [19][31] 78K4 16-bit 16× 8-bit ×4 banks 113 none Macro service available [37]:24,128 78K7 32-bit 16× 16-bit ×16 banks none Macro service available [46] 78K6 16-bit Macro service available 78K1 8-bit 8× 8-bit ×4 banks 64 none For VCR servo controls [40]:3,39 78K3 16-bit 16× 8-bit ×8 banks 113–115 none Macro service available [47]:3–28,45 78K2 8-bit 8× 8-bit ×4 banks 65 none General purpose [44]:16,50 87AD 8-bit 8× 8-bit ×2 banks CMOS: 159NMOS: 158 none Predecessor of 78K [45]:21,39 (17K) 4-bit 128× 4-bit ×2 banks 47 none Predecessor of 178K [30] RL78 NEC V20 V850 Renesas 740 IEBus ^ Oklobdzija, Vojin G. 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CiteSeerX 10.1.1.676.6935. ISBN 978-1-61208-379-7. ISSN 2308-426X. ^ a b Renesas official: 78K0R Microcontrollers User's Manual: Instructions. Renesas Electronics. ^ a b Renesas official: RL78 family User's Manual: Software. Renesas Electronics. ^ a b c 17K 4-bit Microcontroller Data Book (1992). NEC. ^ a b Renesas official: UPD178024 Subseries User's Manual. Renesas Electronics. ^ a b Renesas official: UPD179327 Subseries User's Manual. Renesas Electronics. ^ JPRS Report: Science & technology. Japan. Foreign Broadcast Information Service. 1994. p. 25. The 78K/IV has upward compatibility regarding the instruction sets of the existing 78K/0, 78K/II and 78K/III. Major features of the 78K/IV are: 1) linear addressing of 16 M bytes, 2) wide operative voltage = 2.7-6.0 V, 3) efficient power management, 4) instruction sets for C compiler. NEC has developed the 1st product "puPD784026 subseries" that has upward-compatible peripheral functions of the 78K/II series. ^ Ohuchi, Mitsurou; Kawata, Kazuhide; Akiyama, Shin-ichiro; Imamura, Hirohisa; Fukushima, Kiyoshi; Ishizaki, Norihiko; Imamizu, Jun-ichi; Mori, Takehiko; Ono, Hirohihiko; Nakata, Shigeru (1994). "16ビットシングルチップマイクロコンピュータ78K/4シリーズ (半導体デバイス)" [16-Bit Single Chip Microcomputer 78K/IV Series.]. NEC Technical Journal. 47 (3): 122–127. ^ "NEC: News Release 96/10/30-01". www.nec.co.jp. ^ "Micro Controller (Data Part)". www.cpe.ku.ac.th. ^ a b Renesas official: 78K/IV Series Instructions. Renesas Electronics. ^ Renesas official: UPD784908 Subseries Hardware (Preliminary). Renesas Electronics. ^ Lui, Dr. Gough (16 August 2013). "Salvage: Quantum Fireball 1280Mb AT Hard Drive". Gough's Tech Zone. Phto 2. ^ a b Renesas official: UPD78148 User's Manual. Renesas Electronics. ^ Renesas official: UPD78334 User's Manual. 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Retrieved from " 3 The following pages link to 78K External tools (link count transclusion count sorted list) · See help page for transcluding these entries Showing 50 items. View (previous 50 | next 50) (20 | 50 | 100 | 250 | 500)Intel 80186 (links | edit) Motorola 68HC11 (links | edit) Microcontroller (links | edit) PowerPC (links | edit) Playdia (links | edit) Zilog Z80 (links | edit) Intel MCS-51 (links | edit) Intel MCS-48 (links | edit) ARM architecture family (links | edit) AVR microcontrollers (links | edit) SuperH (links | edit) H8 Family (links | edit) PIC microcontrollers (links | edit) TI MSP430 (links | edit) In-circuit emulation (links | edit) Packard Bell (links | edit) Renesas Electronics (links | edit) NEC (links | edit) NEC V20 (links | edit) JTAG (links | edit) COP8 (links | edit) CompactRISC (links | edit) Zilog eZ80 (links | edit) AMD Am29000 (links | edit) Walter Tenney Carleton (links | edit) Green Rockets Tokatsu (links | edit) MPC5xx (links | edit) Zilog Z8 (links | edit) Sharp NEC Display Solutions (links | edit) ARM7 (links | edit) Kunihiko Iwadare (links | edit) Zenith Data Systems (links | edit) Infineon TriCore (links | edit) In-system programming (links | edit) NEC µPD7720 (links | edit) M32R (links | edit) V850 (links | edit) FR-V (microprocessor) (links | edit) NEC V25 (links | edit) R8C (links | edit) NEC Software Solutions (links | edit) NEC Supertower (links | edit) NEC Cup (links | edit) Comparison of operating system kernels (links | edit) NEC Cup (China) (links | edit) NEC Shun-Ei (links | edit) Atmel ARM-based processors (links | edit) ARM9 (links | edit) Cypress PSoC (links | edit) Tadahiro Sekimoto (links | edit) View (previous 50 | next 50) (20 | 50 | 100 | 250 | 500) Retrieved from " WhatLinksHere/78K" I tried using the Wire library and MPU9250 libraries, but somehow it's not working. Here's what I did: I connected MPU9250 to Arduino Nano 33 BLE via I2C. Then I uploaded this I2C scanner code: #include void setup() { Wire.begin(); Serial.begin(9600); while (!Serial); } void loop() { byte error, address; int nDevices; Serial.println("Scanning..."); nDevices = 0; for(address = 1; address < 127; address++) { Wire.beginTransmission(address); error = Wire.endTransmission(); if (error == 0) { Serial.print("I2C device found at address 0x"); if (address 500) { if (SerialDebug) { // Print acceleration values in milligs! Serial.print("X-acceleration: "); Serial.print(1000 * myIMU.ax); Serial.print(" mg "); // Print gyro values in degree/sec Serial.print("X-gyro rate: "); Serial.print(myIMU.gx, 3); Serial.print(" degrees/sec "); // Print mag values in degree/sec Serial.print("X-mag field: "); Serial.print(myIMU.mx); Serial.print(" mG "); myIMU.tempCount = myIMU.readTempData(); // Read the adc values // Temperature in degrees Centigrade myIMU.temperature = ((float) myIMU.tempCount) / 333.87 + 21.0; } myIMU.count = millis(); } } myIMU.yaw = atan2(2.0f * (*(getQ() + 1) * *(getQ() + 2) + *getQ() * *(getQ() + 3)), *getQ() * *getQ() + * (getQ() + 1) * *(getQ() + 1) - * (getQ() + 2) * *(getQ() + 2) - * (getQ() + 3) * *(getQ() + 3)); myIMU.pitch = -asin(2.0f * (*(getQ() + 1) * *(getQ() + 3) - *getQ() * *(getQ() + 2))); myIMU.roll = atan2(2.0f * (*getQ() * *(getQ() + 1) + * (getQ() + 2) * *(getQ() + 3)), *getQ() * *getQ() - * (getQ() + 1) * *(getQ() + 1) - * (getQ() + 2) * *(getQ() + 2) + * (getQ() + 3) * *(getQ() + 3)); myIMU.pitch *= RAD_TO_DEG; myIMU.yaw *= RAD_TO_DEG; myIMU.yaw -= 8.5; myIMU.roll *= RAD_TO_DEG; if (SerialDebug) { Serial.print("Yaw, Pitch, Roll: "); Serial.print(myIMU.yaw, 2); Serial.print(", "); } myIMU.count = millis(); myIMU.sumCount = 0; myIMU.sum = 0; } // if (myIMU.delt_t > 500) } // if (AHRS) } But after uploading this code, Arduino board is not even getting detected. No serial port is shown. Can you tell what modifications are needed in this code? Share — copy and redistribute the material in any medium or format for any purpose, even commercially. Adapt — remix, transform, and build upon the material for any purpose, even commercially. The licensor cannot revoke these freedoms as long as you follow the license terms. Attribution — You must give appropriate credit , provide a link to the license, and indicate if changes were made . You may do so in any reasonable manner, but not in any way that suggests the licensor endorses you or your use. ShareAlike — If you remix, transform, or build upon the material, you must distribute your contributions under the same license as the original. No additional restrictions — You may not apply legal terms or technological measures that legally restrict others from doing anything the license permits. You do not have to comply with the license for elements of the material in the public domain or where your use is permitted by an applicable exception or limitation . No warranties are given. The license may not give you all of the permissions necessary for your intended use. For example, other rights such as publicity, privacy, or moral rights may limit how you use the material. I just receive my Nano board(s) today and the first thing I wanted to do was map out and explore the I2C sensors on board. I first tried my own I2C_Detector project and it didn't find any devices. I tried using the wire library, bit-banging, re-checked the schematic and tried different pin numbers, but no luck. Then I tried running the standard I2C_scan demo sketch and still nothing. Are there some additional steps needed to access the I2C sensors on this device? I do not have boards yet so take this with a grain of salt. You might take a look at BLE i2c driver source code. For example, GitHub LSM9DS1 Library for Arduino. Contribute to arduino-libraries/Arduino_LSM9DS1 development by creating an account on GitHub. For more Nano BLE drivers, search library manager for "nano ble". The board package can be found by searching board manager for "nano ble". A "Getting started guide" for Nano BLE would be useful. Have you put external pull-ups on the I2C pins? I got it sorted out. I was just trying to use the built-in sensors. Apparently the board has a GPIO pin which controls power to the sensors (for ultra low power mode) and they're on the second I2C bus (Wire1). Hi, have you solved the problem? How to distinguish the two wires on the firmware? You can't perform that action at this time. Family of microcontrollers This article is about the series of AVR microcontrollers. For the AVR instruction set, see Atmel AVR instruction set. Not to be confused with automatic voltage regulator. AVR logo Various older AVR microcontrollers: ATmega8 in 28-pin narrow dual in-line package (DIP-28N), ATxmega128A1 in 100-pin thin quad flat pack (TQFP-100) package, ATtiny45 in 8-pin small outline (SO-8) package ATmega328P in 28-pin narrow dual in-line package (DIP-28N). It is commonly found on Arduino boards. AVR is a family of microcontrollers developed since 1996 by Atmel, acquired by Microchip Technology in 2016. They are 8-bit RISC single-chip microcontrollers based on a modified Harvard architecture. AVR was one of the first microcontroller families to use on-chip flash memory for program storage, as opposed to one-time programmable ROM, EPROM, or EEPROM used by other microcontrollers at the time. AVR microcontrollers are used numerously as embedded systems. They are especially common in hobbyist and educational embedded applications, popularized by their inclusion in many of the Arduino line of open hardware development boards. The AVR 8-bit microcontroller architecture was introduced in 1997. By 2003, Atmel had shipped 500 million AVR flash microcontrollers.[1] The AVR architecture was conceived by two students at the Norwegian Institute of Technology (NTH),[2] Alf-Egil Bogen[3] and Vegard Wollan.[4] Atmel says that the name AVR is not an acronym and does not stand for anything in particular. The creators of the AVR give no definitive answer as to what the term "AVR" stands for.[4] However, it is commonly accepted that AVR stands for Alf and Vegard's RISC processor.[5] Note that the use of "AVR" in this article generally refers to the 8-bit RISC line of Atmel AVR microcontrollers. The original AVR MCU was developed at a local ASIC design company in Trondheim, Norway, called Nordic VLSI at the time, now Nordic Semiconductor, where Bogen and Wollan were working as students.[citation needed] It was known as a µRISC (Micro RISC)[6] and was available as silicon IP/building block from Nordic VLSI.[7] When the technology was sold to Atmel from Nordic VLSI, the internal architecture was further developed by Bogen and Wollan at Atmel Norway, a subsidiary of Atmel. The designers worked closely with compiler writers at IAR Systems to ensure that the AVR instruction set provided efficient compilation of high-level languages.[8] Among the first of the AVR line was the AT90S8515, which in a 40-pin DIP package has the same pinout as an 8051 microcontroller, including the external multiplexed address and data bus. The polarity of the RESET line was opposite (8051's having an active-high RESET, while the AVR has an active-low RESET), but other than that the pinout was identical. The Arduino platform, developed for simple electronics projects, was released in 2005 and featured ATmega8 AVR microcontrollers. The AVR is a modified Harvard architecture machine, where program and data are stored in separate physical memory systems that appear in different address spaces, but having the ability to read data items from program memory using special instructions. AVRs are generally classified into following: tinyAVR – the ATtiny series Main article: ATtiny microcontroller comparison chart Flash size Frequency[MHz] Package SRAM EEPROM 0.5–32 KB 1.6–20 6–32-pin package 32–3072 bytes 64–512 bytes The ATtiny series features small package microcontrollers with a limited peripheral set available. However, the improved tinyAVR 0/1/2-series (released in 2016) include: Peripherals equal to or exceed megaAVR 0-series Event System Improved AVRxt instruction set (improved timing of calls), hardware multiply megaAVR – the ATmega series Flash size Frequency[MHz] Package SRAM EEPROM 4–256 KB 1.6–20 28–100-pin package 256–16384 bytes 256–4096 bytes The ATmega series features microcontrollers that provide an extended instruction set (multiply instructions and instructions for handling larger program memories), an extensive peripheral set, a solid amount of program memory, as well as a wide range of pins available. The megaAVR 0-series (released in 2016) also has functionality such as: Event system New peripherals with enhanced functionality Improved AVRxt instruction set (improved timing of calls) AVR Dx – The AVR Dx family features multiple microcontroller series, focused on HCI, analog signal conditioning and functional safety. Flash size Frequency[MHz] Package SRAM EEPROM Release year 16–128 KB 20–24 at 1.8–5.5 V 14–64-pin package 4–16 KB 512 bytes 2020 The parts numbers is formatted as AVRffDxpp, where ff is flash size, x is family, and pp is number of pins. Example: AVR128DA64 – 64-pin DA-series with 128k flash. All devices in the AVR Dx family include: an Async Type D timer that can run faster than the CPU 12-bit ADC 10-bit DAC AVR DA-series (early 2020) – The high memory density makes these MCUs well suited for both wired and wireless communication-stack-intensive functions. integrated sensors for capacitative touch measurement (HCI) updated core independent peripherals (CIPs) and analog peripherals no external high frequency crystal AVR DB-series (mid-late 2020) – inherits many features from the DA-family, while adding its own: 2 or 3 on-chip opamps MultiVoltage IO (MVIO) on PORTC Supports external HF crystal AVR DD-series 16–64 KiB Flash 2–8 KiB SRAM 14–32-pin package internal 24 MHz oscillator 7–23-channel 130 kS/s 12-bit differential Analog-to-Digital Converter (ADC) no amplifiers 1 analog comparator Two USARTs, one SPI, one dual-mode TWI Multi-Voltage Input/Output (MVIO) support on 3 or 4 pins on Port C 4 Configurable Custom Logic (CCL) cells, 6 Event System channels AVR EA-series 8–64 KiB Flash 28–48-pin package internal 20 MHz oscillator 24–32-channel 130 kS/s 12-bit differential Analog-to-Digital Converter (ADC) Programmable Gain Amplifier (PGA) with up to 16x gain 2 analog comparators Three USARTs, one SPI, one dual-mode TWI no Multi-Voltage Input/Output (MVIO) 4 Configurable Custom Logic (CCL) cells, 6 Event System channels XMEGA Flash size Frequency[MHz] Package SRAM EEPROM Release year 16–256 KB 32 44–100-pin package 1–32 KB 512–2048 bytes — the ATxmega series offers a wide variety of peripherals and functionality such as: Extended performance features, such as DMA, "Event System", and cryptography support Extensive peripheral set with ADCs Application-specific AVR megaAVRs with special features not found on the other members of the AVR family, such as LCD controller, USB controller, advanced PWM, CAN, etc. FPSLIC (AVR with FPGA) FPGA 5k to 40k gates SRAM for the AVR program code, unlike all other AVRs AVR core can run at up to 50 MHz[9] 32-bit AVRsMain article: AVR32 In 2006, Atmel released microcontrollers based on the 32-bit AVR32 architecture. This was a completely different architecture unrelated to the 8-bit AVR, intended to compete with the ARM-based processors. It had a 32-bit data path, SIMD and DSP instructions, along with other audio- and video-processing features. The instruction set was similar to other RISC cores, but it was not compatible with the original AVR (nor any of the various ARM cores). Since then support for AVR32 has been dropped from Linux as of kernel 4.12; compiler support for the architecture in GCC was never mainlined into the compiler's central source-code repository and was available primarily in a vendor-supported fork. At the time that AVR32 was introduced, Atmel had already been a licensee of the ARM architecture, with both ARM7 and ARM9 microcontrollers having been released prior to and concurrently with the AVR32; later Atmel focused most development effort on 32-bit chips with ARM Cortex-M and Cortex-A cores. Atmel ATxmega128A1 in 100-pin TQFP package ATMEL MEGA32U4 die shot The AVRs have 32 single-byte registers and are classified as 8-bit RISC devices. Flash, EEPROM, and SRAM are all integrated onto a single chip, removing the need for external memory in most applications. Some devices have a parallel external bus option to allow adding additional data memory or memory-mapped devices. Almost all devices (except the smallest TinyAVR chips) have serial interfaces, which can be used to connect larger serial EEPROMs or flash chips. Program instructions are stored in non-volatile flash memory. Although the MCUs are 8-bit, each instruction takes one or two 16-bit words. The size of the program memory is usually indicated in the naming of the device itself (e.g., the ATmega64x line has 64 KB of flash, while the ATmega32x line has 32 KB). There is no provision for off-chip program memory; all code executed by the AVR core must reside in the on-chip flash. However, this limitation does not apply to the AT94 FPSLIC AVR/FPGA chips. The data address space consists of the register file, I/O registers, and SRAM. Some small models also map the program ROM into the data address space, but larger models do not. In the tinyAVR and megaAVR variants of the AVR architecture, the working registers are mapped in as the first 32 data memory addresses (000016–001F16), followed by 64 I/O registers (002016–005F16). In devices with many peripherals, these registers are followed by 160 “extended I/O” registers, only accessible as memory-mapped I/O (006016–00FF16). Actual SRAM starts after these register sections, at address 006016 or, in devices with "extended I/O", at 010016. Even though there are separate addressing schemes and optimized opcodes for accessing the register file and the first 64 I/O registers, all can also be addressed and manipulated as if they were in SRAM. The very smallest of the tinyAVR variants use a reduced architecture with only 16 registers (r0 through r15 are omitted) which are not addressable as memory locations. I/O memory begins at address 000016, followed by SRAM. In addition, these devices have slight deviations from the standard AVR instruction set. Most notably, the direct load/store instructions (LDS/STS) have been reduced from 2 words (32 bits) to 1 word (16 bits), limiting the total direct addressable memory (the sum of both I/O and SRAM) to 128 bytes. Conversely, the indirect load instruction's (LD) 16-bit address space is expanded to also include non-volatile memory such as Flash and configuration bits; therefore, the Load Program Memory (LPM) instruction is unnecessary and omitted. (For detailed info, see Atmel AVR instruction set.) In the XMEGA variant, the working register file is not mapped into the data address space; as such, it is not possible to treat any of the XMEGA's working registers as though they were SRAM. Instead, the I/O registers are mapped into the data address space starting at the very beginning of the address space. Additionally, the amount of data address space dedicated to I/O registers has grown substantially to 4096 bytes (000016–0FFF16). As with previous generations, however, the fast I/O manipulation instructions can only reach the first 64 I/O register locations (the first 32 locations for bitwise instructions). Following the I/O registers, the XMEGA series sets aside a 4096 byte range of the data address space, which can be used optionally for mapping the internal EEPROM to the data address space (100016–1FFF16). The actual SRAM is located after these ranges, starting at 200016. Each GPIO port on a tiny or mega AVR drives up to eight pins and is controlled by three 8-bit registers: DDRx, PORTx and PINx, where x is the port identifier. DDRx: Data Direction Register, configures the pins as either inputs or outputs. PORTx: Output port register. Sets the output value on pins configured as outputs. Enables or disables the pull-up resistor on pins configured as inputs. PINx: Input register, used to read an input signal. On some devices, this register can be used for pin toggling: writing a logic one to a PINx bit toggles the corresponding bit in PORTx, irrespective of the setting of the DDRx bit.[10] Newer ATtiny AVRs, like ATtiny817 and its siblings, have their port control registers somewhat differently defined. xmegaAVR have additional registers for push/pull, totem-pole and pullup configurations. Almost all AVR microcontrollers have internal EEPROM for semi-permanent data storage. Like flash memory, EEPROM can maintain its contents when electrical power is removed. In most variants of the AVR architecture, this internal EEPROM memory is not mapped into the MCU's addressable memory space. It can only be accessed the same way an external peripheral device is, using special pointer registers and read/write instructions, which makes EEPROM access much slower than other internal RAM. However, some devices in the SecureAVR (AT90SC) family[11] use a special EEPROM mapping to the data or program memory, depending on the configuration. The XMEGA family also allows the EEPROM to be mapped into the data address space. Since the number of writes to EEPROM is limited – Atmel specifies 100,000 write cycles in their datasheets – a well designed EEPROM write routine should compare the contents of an EEPROM address with desired contents and only perform an actual write if the contents need to be changed. Atmel's AVRs have a two-stage, single-level pipeline design, meaning that the next machine instruction is fetched as the current one is executing. Most instructions take just one or two clock cycles, making AVRs relatively fast among eight-bit microcontrollers. The AVR processors were designed with the efficient execution of compiled C code in mind and have several built-in pointers for the task. Main article: Atmel AVR instruction set The AVR instruction set is more orthogonal than those of most eight-bit microcontrollers, in particular the 8051 clones and PIC microcontrollers with which AVR has competed. However, it is not completely regular: Pointer registers X, Y, and Z have addressing capabilities that are different from each other. Register locations R0 to R15 have more limited addressing capabilities than register locations R16 to R31. I/O ports 0 to 31 can be bit addressed, unlike I/O ports 32 to 63. CLR (clear all bits to zero) affects flags, while SER (set all bits to one) does not, even though they are complementary instructions. (CLR is pseudo-op for EOR R, R; while SER is short for LDI R,$FF. Arithmetic operations such as EOR modify flags, while moves/loads/stores/branches such as LDI do not.) Accessing read-only data stored in the program memory (flash) requires special LPM instructions; the flash bus is otherwise reserved for instruction memory. Some chip-specific differences affect code generation. Code pointers (including return addresses on the stack) are two bytes long on chips with up to 128 KB of flash memory, but three bytes long on larger chips; not all chips have hardware multipliers; chips with over 8 KB of flash have branch and call instructions with longer ranges; and so forth. The mostly regular instruction set makes C (and even Ada) compilers fairly straightforward and efficient. GCC has included AVR support for quite some time, and that support is widely used. LLVM also has rudimentary AVR support. In fact, Atmel solicited input from major developers of compilers for small microcontrollers, to determine the instruction set features that were most useful in a compiler for high-level languages.[8] The AVR line can normally support clock speeds from 0 to 20 MHz, with some devices reaching 32 MHz. Lower-powered operation usually requires a reduced clock speed. All recent (Tiny, Mega, and Xmega, but not 90S) AVRs feature an on-chip oscillator, removing the need for external clocks or resonator circuitry. Some AVRs also have a system clock prescaler that can divide down the system clock by up to 1024. This prescaler can be reconfigured by software during run-time, allowing the clock speed to be optimized. Since all operations (excluding multiplication and 16-bit add/subtract) on registers R0–R31 are single-cycle, the AVR can achieve up to 1 MIPS per MHz, i.e. an 8 MHz processor can achieve up to 8 MIPS. Loads and stores to/from memory take two cycles, branching takes two cycles. Branches in the latest "3-byte PC" parts such as ATmega2560 are one cycle slower than on previous devices. AVRs have a large following due to the free and inexpensive development tools available, including reasonably priced development boards and free development software. The AVRs are sold under various names that share the same basic core, but with different peripheral and memory combinations. Compatibility between chips in each family is fairly good, although I/O controller features may vary. The Atmel AVR GNU C/C++ cross compiler, "avr-gcc" and "avr-g++", is used in both WinAVR and Atmel Studio.[12][13][14][15][16] The Arduino team borrowed from WinAVR for the Windows version of the Arduino software.[17] See external links for sites relating to AVR development. AVRs offer a wide range of features: Multifunction, bi-directional general-purpose I/O ports with configurable, built-in pull-up resistors Multiple internal oscillators, including RC oscillator without external parts Internal, self-programmable instruction flash memory up to 256 KB (384 KB on XMega) In-system programmable using serial/parallel low-voltage proprietary interfaces or JTAG Optional boot code section with independent lock bits for protection On-chip debugging (OCD) support through JTAG or debugWIRE on most devices The JTAG signals (TMS, TDI, TDO, and TCK) are multiplexed on GPIOs. These pins can be configured to function as JTAG or GPIO depending on the setting of a fuse bit, which can be programmed via in-system programming (ISP) or HVSP. By default, AVRs with JTAG come with the JTAG interface enabled. debugWIRE uses the /RESET pin as a bi-directional communication channel to access on-chip debug circuitry. It is present on devices with lower pin counts, as it only requires one pin. Internal data EEPROM up to 4 KB Internal SRAM up to 16 KB (32 KB on XMega) External 64 KB little endian data space on certain models, including the Mega8515 and Mega162. The external data space is overlaid with the internal data space, such that the full 64 KB address space does not appear on the external bus and accesses to e.g. address 010016 will access internal RAM, not the external bus. In certain members of the XMega series, the external data space has been enhanced to support both SRAM and SDRAM. As well, the data addressing modes have been expanded to allow up to 16 MB of data memory to be directly addressed. 8-bit and 16-bit timers PWM output (some devices have an enhanced PWM peripheral which includes a dead-time generator) Input capture that record a time stamp triggered by a signal edge analog comparator 10 or 12-bit A/D converters, with multiplex of up to 16 channels 12-bit D/A converters A variety of serial interfaces, including I^{2}C compatible Two-Wire Interface (TWI) Synchronous/asynchronous serial peripherals (UART/USART) (used with RS-232, RS-485, and more) Serial Peripheral Interface Bus (SPI) Universal Serial Interface (USI): a multi-purpose hardware communication module that can be used to implement an SPI,[18] I2C[19][20] or UART[21] interface. Brownout detection Watchdog timer (WDT) Multiple power-saving sleep modes Lighting and motor control (PWM-specific) controller models CAN controller support USB controller support Proper full-speed (12 Mbit/s) hardware & Hub controller with embedded AVR. Also freely available low-speed (1.5 Mbit/s) (HID) bitbanging software emulations Ethernet controller support LCD controller support Low-voltage devices operating down to 1.8 V (to 0.7 V for parts with built-in DC–DC upconverter) picoPower devices DMA controllers and "event system" peripheral communication. Fast cryptography support for AES and DES There are many means to load program code into an AVR chip. The methods to program AVR chips varies from AVR family to family. Most of the methods described below use the RESET line to enter programming mode. In order to avoid the chip accidentally entering such mode, it is advised to connect a pull-up resistor between the RESET pin and the positive power supply.[22] 6- and 10-pin ISP header diagrams The in-system programming (ISP) programming method is functionally performed through SPI, plus some twiddling of the Reset line. As long as the SPI pins of the AVR are not connected to anything disruptive, the AVR chip can stay soldered on a PCB while reprogramming. All that is needed is a 6-pin connector and programming adapter. This is the most common way to develop with an AVR. The Atmel-ICE device or AVRISP mkII (Legacy device) connects to a computer's USB port and performs in-system programming using Atmel's software. AVRDUDE (AVR Downloader/UploaDEr) runs on Linux, FreeBSD, Windows, and Mac OS X, and supports a variety of in-system programming hardware, including Atmel AVRISP mkII, Atmel JTAG ICE, older Atmel serial-port based programmers, and various third-party and "do-it-yourself" programmers.[23] The Program and Debug Interface (PDI) is an Atmel proprietary interface for external programming and on-chip debugging of XMEGA devices. The PDI supports high-speed programming of all non-volatile memory (NVM) spaces; flash, EEPROM, fuses, lock-bits and the User Signature Row. This is done by accessing the XMEGA NVM controller through the PDI interface, and executing NVM controller commands. The PDI is a 2-pin interface using the Reset pin for clock input (PDI_CLK) and a dedicated data pin (PDI_DATA) for input and output.[24] The Unified Program and Debug Interface (UPDI) is a one-wire interface for external programming and on-chip debugging of newer ATtiny and ATmega devices. UPDI chips can be programmed by an Atmel-ICE, a PICkit 4, an Arduino (flashed with jtag2updi),[25] or though a UART (with a 1 kΩ resistor between the TX and RX pins) controlled by Microchip's Python utility pymcuprog.[26] High-voltage serial programming (HVSP)[27] is mostly the backup mode on smaller AVRs. An 8-pin AVR package does not leave many unique signal combinations to place the AVR into a programming mode. A 12-volt signal, however, is something the AVR should only see during programming and never during normal operation. The high voltage mode can also be used in some devices where the reset pin was disabled by fuses. High-voltage parallel programming (HVPP) is considered the "final resort" and may be the only way to correct bad fuse settings on an AVR chip. Most AVR models can reserve a bootloader region, 256 bytes to 4 KB, where re-programming code can reside. At reset, the bootloader runs first and does some user-programmed determination whether to re-program or to jump to the main application. The code can re-program through any interface available, or it could read an encrypted binary through an Ethernet adapter like PXE. Atmel has application notes and code pertaining to many bus interfaces.[28][29][30][31] The AT90SC series of AVRs are available with a factory mask-ROM for program memory, instead of flash.[32] Because of the large up-front cost and minimum order quantity, a mask-ROM is only cost-effective for high-production runs. aWire is a new one-wire debug interface available on the new UC3L AVR32 devices. The AVR offers several options for debugging, mostly involving on-chip debugging while the chip is in the target system. Main article: debugWIRE debugWIRE is Atmel's solution for providing on-chip debug capabilities via a single microcontroller pin. It is useful for lower pin-count parts which cannot provide the four "spare" pins needed for JTAG. The JTAGICE mkII, mkIII and the AVR Dragon support debugWIRE. debugWIRE was developed after the original JTAGICE release, and now clones support it. The Joint Test Action Group (JTAG) feature provides access to on-chip debugging functionality while the chip is running in the target system.[33] JTAG allows accessing internal memory and registers, setting breakpoints on code, and single-stepping execution to observe system behaviour. Atmel provides a series of JTAG adapters for the AVR: The Atmel-ICE[34] is the latest adapter. It supports JTAG, debugWire, aWire, SPI, TPI, and PDI interfaces. The JTAGICE 3[35] is a midrange debugger in the JTAGICE family (JTAGICE mkIII). It supports JTAG, aWire, SPI, and PDI interfaces. The JTAGICE mkII[36] replaces the JTAGICE and is similarly priced. The JTAGICE mkII interfaces to the PC via USB, and supports both JTAG and the newer debugWIRE interface. Numerous third-party clones of the Atmel JTAGICE mkII device started shipping after Atmel released the communication protocol.[37] The AVR Dragon[38] is a low-cost (approximately $50) substitute for the JTAGICE mkII for certain target parts. The AVR Dragon provides in-system serial programming, high-voltage serial programming and parallel programming, as well as JTAG or debugWIRE emulation for parts with 32 KB of program memory or less. ATMEL changed the debugging feature of AVR Dragon with the latest firmware of AVR Studio 4 – AVR Studio 5 and now it supports devices over 32 KB of program memory. The JTAGICE adapter interfaces to the PC via a standard serial port.[39] Although the JTAGICE adapter has been declared "end-of-life" by Atmel, it is still supported in AVR Studio and other tools. JTAG can also be used to perform a boundary scan test,[40] which tests the electrical connections between AVRs and other boundary scan capable chips in a system. Boundary scan is well-suited for a production line, while the hobbyist is probably better off testing with a multimeter or oscilloscope. Atmel STK500 development board Official Atmel AVR development tools and evaluation kits contain a number of starter kits and debugging tools with support for most AVR devices: The STK600 starter kit and development system is an update to the STK500.[41] The STK600 uses a base board, a signal routing board, and a target board. The base board is similar to the STK500, in that it provides a power supply, clock, in-system programming, an RS-232 port and a CAN (Controller Area Network, an automotive standard) port via DE9 connectors, and stake pins for all of the GPIO signals from the target device. The target boards have ZIF sockets for DIP, SOIC, QFN, or QFP packages, depending on the board. The signal routing board sits between the base board and the target board, and routes the signals to the proper pin on the device board. There are many different signal routing boards that could be used with a single target board, depending on what device is in the ZIF socket. The STK600 allows in-system programming from the PC via USB, leaving the RS-232 port available for the target microcontroller. A 4 pin header on the STK600 labeled 'RS-232 spare' can connect any TTL level USART port on the chip to an onboard MAX232 chip to translate the signals to RS-232 levels. The RS-232 signals are connected to the RX, TX, CTS, and RTS pins on the DB-9 connector. The STK500 starter kit and development system features ISP and high voltage programming (HVP) for all AVR devices, either directly or through extension boards. The board is fitted with DIP sockets for all AVRs available in DIP packages. STK500 Expansion Modules: Several expansion modules are available for the STK500 board: STK501 – Adds support for microcontrollers in 64-pin TQFP packages. STK502 – Adds support for LCD AVRs in 64-pin TQFP packages. STK503 – Adds support for microcontrollers in 100-pin TQFP packages. STK504 – Adds support for LCD AVRs in 100-pin TQFP packages. STK505 – Adds support for 14 and 20-pin AVRs. STK520 – Adds support for 14 and 20, and 32-pin microcontrollers from the AT90PWM and ATmega family. STK524 – Adds support for the ATmega32M1/C1 32-pin CAN/LIN/Motor Control family. STK525 – Adds support for the AT90USB microcontrollers in 64-pin TQFP packages. STK526 – Adds support for the AT90USB microcontrollers in 32-pin TQFP packages. The STK200 starter kit and development system has a DIP socket that can host an AVR chip in a 40, 20, or 8-pin package. The board has a 4 MHz clock source, 8 light-emitting diode (LED)s, 8 input buttons, an RS-232 port, a socket for a 32 KB SRAM and numerous general I/O. The chip can be programmed with a dongle connected to the parallel port. Supported microcontrollers (according to the manual) Chip Flash size EEPROM SRAM Frequency[MHz] Package AT90S1200 1 KB 64 B 0 B 12 PDIP-20 AT90S2313 2 KB 128 B 128 B 10 PDIP-20 AT90S/LS2323 2 KB 128 B 128 B 10 PDIP-8 AT90S/LS2343 2 KB 128 B 128 B 10 PDIP-8 AT90S4414 4 KB 256 B 256 B 8 PDIP-40 AT90S/LS4434 4 KB 256 B 256 B 8 PDIP-40 AT90S8515 8 KB 512 B 512 B 8 PDIP-40 AT90S/LS8535 8 KB 512 B 512 B 8 PDIP-40 The Atmel ICE is the currently supported inexpensive tool to program and debug all AVR devices (unlike the AVRISP/AVRISP mkII, Dragon, etc. discussed below). It connects to and receives power from a PC via USB, and supports JTAG, PDI, aWire, debugWIRE, SPI, SWD, TPI, and UPDI (the Microchip Unified Program and Debug Interface) interfaces. The ICE can program and debug all AVRs via the JTAG interface, and program with additional interfaces as supported on each device: 8-bit AVR XMEGA devices via the PDI 2-wire interface 8-bit megaAVR and tinyAVR devices via SPI for all with OCD (on-chip debugger) support 8-bit tinyAVR microcontrollers with TPI support 32-bit SAM Arm Cortex-M based microcontrollers via SWD Target operating voltage ranges of 1.62V to 5.5V are supported as well as the following clock ranges: Supports JTAG & PDI clock frequencies from 32 kHz to 7.5 MHz Supports aWire baud rates from 7.5 kbit/s to 7 Mbit/s Supports debugWIRE baud rates from 4 kbit/s to 0.5 Mbit/s Supports SPI clock frequencies from 8 kHz to 5 MHz Supports SWD clock frequencies from 32 kHz to 2 MHz The ICE is supported by the Microchip Studio IDE, as well as a command line interface (atprogram). The Atmel-ICE supports a limited implementation of the Data Gateway Interface (DGI) when debugging and programming features are not in use. The Data Gateway Interface is an interface for streaming data from a target device to the connected computer. This is meant as a useful adjunct to the unit to allow for demonstration of application features and as an aid in application level debugging. AVRISP mkII The AVRISP and AVRISP mkII are inexpensive tools allowing all AVRs to be programmed via ICSP. The AVRISP connects to a PC via a serial port and draws power from the target system. The AVRISP allows using either of the "standard" ICSP pinouts, either the 10-pin or 6-pin connector. The AVRISP mkII connects to a PC via USB and draws power from USB. LEDs visible through the translucent case indicate the state of target power. As the AVRISP mkII lacks driver/buffer ICs,[42] it can have trouble programming target boards with multiple loads on its SPI lines. In such occurrences, a programmer capable of sourcing greater current is required. Alternatively, the AVRISP mkII can still be used if low-value (~150 ohm) load-limiting resistors can be placed on the SPI lines before each peripheral device. Both the AVRISP and the AVRISP mkII are now discontinued, with product pages removed from the Microchip website. As of July 2019 the AVRISP mkII is still in stock at a number of distributors. There are also a number of 3rd party clones available. AVR Dragon with ISP programming cable and attached, blue/greenish ZIF Socket The Atmel Dragon is an inexpensive tool which connects to a PC via USB. The Dragon can program all AVRs via JTAG, HVP, PDI,[43] or ICSP. The Dragon also allows debugging of all AVRs via JTAG, PDI, or debugWire; a previous limitation to devices with 32 KB or less program memory has been removed in AVR Studio 4.18.[44] The Dragon has a small prototype area which can accommodate an 8, 28, or 40-pin AVR, including connections to power and programming pins. There is no area for any additional circuitry, although this can be provided by a third-party product called the "Dragon Rider".[45] The JTAG In Circuit Emulator (JTAGICE) debugging tool supports on-chip debugging (OCD) of AVRs with a JTAG interface. The original JTAGICE (sometimes retroactively referred to as JTAGICE mkI) uses an RS-232 interface to a PC and can only program AVRs with a JTAG interface. The JTAGICE mkI is no longer in production, however it has been replaced by the JTAGICE mkII. The JTAGICE mkII debugging tool supports on-chip debugging (OCD) of AVRs with SPI, JTAG, PDI, and debugWIRE interfaces. The debugWire interface enables debugging using only one pin (the Reset pin), allowing debugging of applications running on low pin-count microcontrollers. The JTAGICE mkII connects using USB, but there is an alternate connection via a serial port, which requires using a separate power supply. In addition to JTAG, the mkII supports ISP programming (using 6-pin or 10-pin adapters). Both the USB and serial links use a variant of the STK500 protocol. The JTAGICE3 updates the mkII with more advanced debugging capabilities and faster programming. It connects via USB and supports the JTAG, aWire, SPI, and PDI interfaces.[46] The kit includes several adapters for use with most interface pinouts. The AVR ONE! is a professional development tool for all Atmel 8-bit and 32-bit AVR devices with On-Chip Debug capability. It supports SPI, JTAG, PDI, and aWire programming modes and debugging using debugWIRE, JTAG, PDI, and aWire interfaces.[47] Atmel ATmega169 in 64-pad MLF package on the back of an Atmel AVR Butterfly board Main article: AVR Butterfly The very popular AVR Butterfly demonstration board is a self-contained, battery-powered computer running the Atmel AVR ATmega169V microcontroller. It was built to show off the AVR family, especially a then new built-in LCD interface. The board includes the LCD screen, joystick, speaker, serial port, real time clock (RTC), flash memory chip, and both temperature and voltage sensors. Earlier versions of the AVR Butterfly also contained a CdS photoresistor; it is not present on Butterfly boards produced after June 2006 to allow RoHS compliance.[48] The small board has a shirt pin on its back so it can be worn as a name badge. The AVR Butterfly comes preloaded with software to demonstrate the capabilities of the microcontroller. Factory firmware can scroll your name, display the sensor readings, and show the time. The AVR Butterfly also has a piezoelectric transducer that can be used to reproduce sounds and music. The AVR Butterfly demonstrates LCD driving by running a 14-segment, six alpha-numeric character display. However, the LCD interface consumes many of the I/O pins. The Butterfly's ATmega169 CPU is capable of speeds up to 8 MHz, but it is factory set by software to 2 MHz to preserve the button battery life. A pre-installed bootloader program allows the board to be re-programmed via a standard RS-232 serial plug with new programs that users can write with the free Atmel IDE tools. This small board, about half the size of a business card, is priced at slightly more than an AVR Butterfly. It includes an AT90USB1287 with USB On-The-Go (OTG) support, 16 MB of DataFlash, LEDs, a small joystick, and a temperature sensor. The board includes software, which lets it act as a USB mass storage device (its documentation is shipped on the DataFlash), a USB joystick, and more. To support the USB host capability, it must be operated from a battery, but when running as a USB peripheral, it only needs the power provided over USB. Only the JTAG port uses conventional 2.54 mm pinout. All the other AVR I/O ports require more compact 1.27 mm headers. The AVR Dragon can both program and debug since the 32 KB limitation was removed in AVR Studio 4.18, and the JTAGICE mkII is capable of both programming and debugging the processor. The processor can also be programmed through USB from a Windows or Linux host, using the USB "Device Firmware Update" protocols. Atmel ships proprietary (source code included but distribution restricted) example programs and a USB protocol stack with the device. LUFA[49] is a third-party free software (MIT license) USB protocol stack for the USBKey and other 8-bit USB AVRs. The RAVEN kit supports wireless development using Atmel's IEEE 802.15.4 chipsets, for Zigbee and other wireless stacks. It resembles a pair of wireless more-powerful Butterfly cards, plus a wireless USBKey; and costing about that much (under $US100). All these boards support JTAG-based development. The kit includes two AVR Raven boards, each with a 2.4 GHz transceiver supporting IEEE 802.15.4 (and a freely licensed Zigbee stack). The radios are driven with ATmega1284p processors, which are supported by a custom segmented LCD driven by an ATmega3290p processor. Raven peripherals resemble the Butterfly: piezo speaker, DataFlash (bigger), external EEPROM, sensors, 32 kHz crystal for RTC, and so on. These are intended for use in developing remote sensor nodes, to control relays, or whatever is needed. The USB stick uses an AT90USB1287 for connections to a USB host and to the 2.4 GHz wireless links. These are intended to monitor and control the remote nodes, relying on host power rather than local batteries. A wide variety of third-party programming and debugging tools are available for the AVR. These devices use various interfaces, including RS-232, PC parallel port, and USB.[50] Atmel AVR ATmega328 28-pin DIP on an Arduino Duemilanove board Atmel AVR ATmega8 28-pin DIP on a custom development board AVRs have been used in various automotive applications such as security, safety, powertrain and entertainment systems. Atmel has recently launched a new publication "Atmel Automotive Compilation" to help developers with automotive applications. Some current usages are in BMW, Daimler-Chrysler and TRW. The Arduino physical computing platform is based on an ATmega328 microcontroller (ATmega168 or ATmega8 in board versions older than the Diecimila). The ATmega1280 and ATmega2560, with more pinout and memory capabilities, have also been employed to develop the Arduino Mega platform. Arduino boards can be used with its language and IDE, or with more conventional programming environments (C, assembler, etc.) as just standardized and widely available AVR platforms. USB-based AVRs have been used in the Microsoft Xbox hand controllers. The link between the controllers and Xbox is USB. Numerous companies produce AVR-based microcontroller boards intended for use by hobbyists, robot builders, experimenters and small system developers including: Cubloc,[51] gnusb,[52] BasicX,[53] Oak Micros,[54] ZX Microcontrollers,[55] and myAVR.[56] There is also a large community of Arduino-compatible boards supporting similar users. Schneider Electric used to produce the M3000 Motor and Motion Control Chip, incorporating an Atmel AVR Core and an advanced motion controller for use in a variety of motion applications but this has been discontinued.[57] With the growing popularity of FPGAs among the open source community, people have started developing open source processors compatible with the AVR instruction set. The OpenCores website lists the following major AVR clone projects: pAVR,[58] written in VHDL, is aimed at creating the fastest and maximally featured AVR processor, by implementing techniques not found in the original AVR processor such as deeper pipelining. avr_core,[59] written in VHDL, is a clone aimed at being as close as possible to the ATmega103. Navré,[60] written in Verilog, implements all Classic Core instructions and is aimed at high performance and low resource usage. It does not support interrupts. softavrcore,[61] written in Verilog, implements the AVR instruction set up to AVR5, supports interrupts along with optional automatic interrupt acknowledgement, power saving via sleep mode plus some peripheral interfaces and hardware accelerators (such as UART, SPI, cyclic redundancy check calculation unit and system timers). These peripherals demonstrate how could these be attached and configured for this core. Within the package, a full-featured FreeRTOS port is also available as an example for the core + peripheral utilization. The opencores project CPU lecture[62] written in VHDL by Dr. Jürgen Sauermann explains in detail how to design a complete AVR-based system on a chip (SoC). In addition to the chips manufactured by Atmel, clones are available from LogicGreen Technologies.[63] These parts are not exact clones - they have a few features not found in the chips they are "clones" of, and higher maximum clock speeds, but use SWD (Serial Wire Debug, a variant of JTAG from ARM) instead of ISP for programming, so different programming tools must be used. Microcontrollers using the ATmega architecture are being manufactured by NIIET in Voronezh, Russia, as part of the 1887 series of integrated circuits. This includes an ATmega128 under the designation 1887VE7T (Russian: 1887ВЕ7Т).[64] ^ Atmel press release. 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The Wikibook Embedded Systems has a page on the topic of: Atmel AVR Electronics portal Official Website Atmel AVR Official Community AVR Freaks community Microchip Forum Pinout Diagrams AVR DIP-Packages: ATtiny44/45/84/85, ATmega8, ATmega644P, ATmega1284P AVR SMD-Packages: ATmega328, ATmega2560, ATmega32U4 Simulators AVR8js (8-bit in-browser simulator) Retrieved from " 2Microcontroller family 78K Family microcontrollersGeneral informationLaunched1986; 39 years ago(1986)DiscontinuedcurrentCommon manufacturerRenesas Electronics(formerly NEC)PerformanceMax. CPU clock rate32 kHz to 24 MHzData width8/16Address width20/24[1]ArchitectureInstruction set78K FamilyPhysical specificationsCores1Products, models, variantsVariant78K0R, 78K0S, 78K0, 78K4, 78K6, 78K3, 78K7, 78K1, 78K2HistoryPredecessor87AD Family, 17K FamilySuccessorRL78 Family V850 Family 78K0/KX1+ Do It board (with in-circuit emulator, MINICUBE) 78K0R/KG3 Cool It board with in-circuit emulator, IECUBE (formerly, MINICUBE2) 78K is the trademark name of 16- and 8-bit microcontroller family manufactured by Renesas Electronics, originally developed by NEC[3][4]:229 started in 1986.[5]:7,line 2 The basis of 78K Family is an accumulator-based register-bank CISC architecture. 78K is a single-chip microcontroller, which usually integrates; program ROM, data RAM, serial interfaces, timers, I/O ports, an A/D converter, an interrupt controller, and a CPU core, on one die.[6][7]:412 Its application area is mainly simple mechanical system controls and man-machine interfaces.[8][9][10] Regarding software development tools, C compilers and macro-assemblers are available.[11]:99 As for development tool hardware, full probing-pod type and debug port type in-circuit emulators,[12][13] and flash ROM programmers[14]:22-24 are available. Historically, the family has 11 series with 9 instruction set architectures. As of 2018, 3 instruction set architectures, those are 8-bit 78K0, 8-bit 78K0S, and 16-bit 78K0R, are still promoted for customers' new designs.[14] But in most of cases, migration to RL78 Family,[15] which is a successor of 78K0R and almost binary level compatible with 78K0R,[16]:20 is recommended.[17] 78K0 Series (as [ja]) (also known as 78K/0) is a long-running 8-bit accumulator-based register-bank CISC architecture. It has the basis of 78K0S and 78K0R Series. It contains 8× 8-bit registers ×4 banks. In addition to 8-bit accumulator-based operations, it performs ALU operation twice. Each instructions are performed serially without instruction pipelining. It has 16-bit 64K Byte address space.[18][19][20] Some variants of 78K0 have affordable and compact type 8-bit R-2R D/A converter, which does not have monotonicity because it is not trimmed for adjustment nor followed by operational amplifier. In its earlier stage, the Program Memory was one-time PROM (OTP), UV-EPROM, or mask ROM.[20] But with the times, it became flash memory.[21][22] 78K0S Series (also known as 78K/0S) is a low-end version of 78K0.[23][24][25] It has 8× 8-bit registers without any banks. In addition, some instructions, such as multiplication and division, are removed from 78K0 instruction set architecture.[26] 78K0R Series is a 16-bit single-chip microcontroller with 3-stage instruction pipelining.[27] Its instruction set is similar to 78K0 and covers 16- and 8-bit operations. It has 20-bit 1M Byte address space.[28] 75 instructions out of 80 are identical with that of RL78 Family. Its successor is RL78.[16]:20[15][29] 178K0S Series (also known as 178K/0S) is a successor of 17K Family with 78K0S core for DTS (Digital Tuning Systems) and remote controls.[30] It integrates 17K family's peripheral functions with 78K0 8-bit CPU core on a single chip.[31] 178K0S Series (also known as 178K/0S) is a successor of 17K Family with the 78K0S CPU core.[30] 78K4 Series (also known as 78K/4) is a 16-bit single-chip microcontroller with 16- and 8-bit operations.[33][34][35][36] It has 16× 8-bit registers ×4 banks, which can be also used for 8× 16-bit registers ×4 banks. Some of these registers can be also used as 24-bit extension for addressing modes.[37] It has 24-bit 16M Byte address space. It has microcode-based operations named Macro Service with interrupt functions.[38]:§23.8,560–593 78K7 Series (also known as 78K/7) is a 32-bit single-chip microcontroller with 32, 16 and 8 bit operations. It has 16× 16-bit registers ×16 banks, and 16× 8-bit registers ×16 banks. It has microcode-based operations named Macro Service with interrupt functions. It has 24-bit 16M Byte linear address space. It is used for some Quantum Fireball products,[39]Photo 2 but shortly replaced with V850 Family 32-bit RISC microcontrollers. 78K6 Series (also known as 78K/6) is a 16-bit single-chip microcontroller with 16 and 8 bit operations. Its life-time was short, and less variants. 78K1 Series (also known as 78K/1) is an 8-bit single-chip microcontroller. It has 8× 8-bit registers ×4 banks. 78K1 series is used for various consumer products such as Televisions and video cassette recorders. μPD78148 sub-series integrates 2 operational amplifiers.[40] 78K3 Series (also known as 78K/3) is a 16-bit single-chip microcontroller with 16 and 8 bit operations. It has 16× 8-bit registers ×8 banks, which can be also used for 8× 16-bit registers ×8 banks. Its address space is 16-bit 64K Byte. It is developed as high-end series of 78K Family. It has microcode-based operations named Macro Service with interrupt functions.[41]:§13.4,261–280 This series is used for some hard disk drives, especially Quantum Fireball Series products.[42] μPD78364 sub-series is used for inverter compressor controls.[43] It is also used for traction control systems of some cars. 78K2 Series (also known as 78K/2) is an 8-bit single-chip microcontroller. It has 8× 8-bit registers ×4 banks. It is developed as general purpose series of 78K Family.[44] 87AD Family[4]:229 is an 8-bit single-chip microcontroller. It has 8× 8-bit registers ×4 banks. Its instruction set architecture became the basis of 78K.[45] 17K Family[4]:229 is a 4-bit single-chip microcontroller, especially dedicated for DTS (Digital Tuning Systems) and remote controls. It has 2 plane of 128× 4-bit registers, and sophisticated fully orthogonal instruction set. This instruction set is completely different from that of 78K Family.[30] Series ALU Registers Instructions Pipeline Remark Documents 87AD 8-bit 8× 8-bit ×4 banks 80 (75+5) 4-stage Successor of 78K0R [29] 8 RL78-S2 16-bit 8× 8-bit ×4 banks 75 (75+3) 3-stage RL78-S1 8-bit 8× 8-bit ×4 banks 74 (75-1) 3-stage 78K0R 16-bit 8× 8-bit ×4 banks 80 3-stage Extended 78K0 [28] 18 78K0S 8-bit 8× 8-bit (no bank) 47 none Simplified 78K0 [25] 78K0 8-bit 8× 8-bit ×4 banks 48 none Basic 78K0 core [19] 178K0S 8-bit 8× 8-bit 47 none 78K0S for DTS;Digital Tuning System [25][32] 178K0 8-bit 8× 8-bit ×4 banks 48 none 78K0 for DTS [31] 78K4 16-bit 16× 8-bit ×4 banks 113 none Macro service available [37]:24,128 78K7 32-bit 16× 16-bit ×16 banks none Macro service available [46] 78K6 16-bit Macro service available 78K1 8-bit 8× 8-bit ×4 banks 64 none For VCR servo controls [40]:3,39 78K3 16-bit 16× 8-bit ×8 banks 113–115 none Macro service available [47]:3–28,45 78K2 8-bit 8× 8-bit ×4 banks 60 none General purpose [44]:16,50 87AD 8-bit 8× 8-bit ×4 banks 42 none Predecessor of 78K [45]:21,39 (17K) 4-bit 128× 4-bit ×2 banks 47 none Predecessor of 178K [30] RL78 NEC V20 V850 Renesas 740 IEBus ^ Oklobdzija, Vojin G. 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View (previous 50 | next 50) (20 | 50 | 100 | 250 | 500)Intel 80186 (links | edit) Motorola 68HC11 (links | edit) PowerPC (links | edit) Zilog Z80 (links | edit) MCS-51 (links | edit) Intel MCS-48 (links | edit) ARM architecture family (links | edit) SuperH (links | edit) H8 Family (links | edit) PIC microcontrollers (links | edit) TI MSP430 (links | edit) Packard Bell (links | edit) NEC (links | edit) NEC V20 (links | edit) JTAG (links | edit) CompactRISC (links | edit) Zilog eZ80 (links | edit) AMD Am29000 (links | edit) Walter Tenney Carleton (links | edit) Green Rockets Tokatsu (links | edit) MPC5xx (links | edit) Zilog Z8 (links | edit) Sharp NEC Display Solutions (links | edit) ARM7 (links | edit) Kunihiko Iwadare (links | edit) Zenith Data Systems (links | edit) Infineon TriCore (links | edit) In-system programming (links | edit) NEC μPD7720 (links | edit) M32R (links | edit) V850 (links | edit) FR-V (microprocessor) (links | edit) NEC V25 (links | edit) NEC V60 (links | edit) NEC Software Solutions (links | edit) NEC Supertower (links | edit) NEC Cup (China) (links | edit) NEC Shun-Ei (links | edit) ARM Ltd. (links | edit) Atmel ARM-based processors (links | edit) ARM9 (links | edit) Cypress PSoC (links | edit) Tadahiro Sekimoto (links | edit) View (previous 50 | next 50) (20 | 50 | 100 | 250 | 500) Retrieved from " WhatLinksHere/78K". the free encyclopedia that anyone can edit. 107,583 active editors 7,025,415 articles in English Sir William Gordon-Cumming (20 July 1848 – 20 May 1930) was a Scottish landowner, soldier and socialite. He was the central figure in the royal baccarat scandal of 1891. He joined the British Army in 1868 and saw service in South Africa, Egypt and Sudan; he was also a keen hunter and travelled in the US and India. A friend of Edward, Prince of Wales, for over 20 years, in 1890 he attended a house party at Tranby Croft, where he took part in a game of baccarat at the behest of the prince. During the course of two nights' play he was accused of cheating, which he denied. After news of the affair leaked out, he sued five members of the party for slander; Edward was called as a witness. The case was a public spectacle in the UK and abroad, but the verdict went against Gordon-Cumming and he was ostracised from polite society. After the court case he married an American heiress, but their relationship was unhappy. (Full article...) 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Ongoing: Gaza war Russian invasion of Ukraine timeline Sudanese civil war timeline Recent deaths: Andrea Gibson Raymond Cole Felix Baumgartner Faqia Singh Bradley John Murdoch Frank Barrie Nominate an article July 20 Forensic experts at the site of the Suruç bombing 1807 – French brothers Claude and Nicéphore Niépce received a patent for their Pyréolophore, one of the world's first internal combustion engines. 1951 – Abdullah I of Jordan was assassinated while visiting the Al-Aqsa Mosque in Jerusalem. 1976 – The Viking 1 lander became the first spacecraft to successfully land on Mars and perform its mission. 1997 – USS Constitution, one of the United States Navy's original six frigates, sailed for the first time in 116 years after a full restoration. 2015 – A suicide attack (aftermath pictured) in Suruç, Turkey, for which Islamic State of Iraq and the Levant (ISIL) claimed responsibility, killed 34 people and injured 104 others. Alexander the Great (b. 356 BC)Amanda Clement (d. 1971)Bruce Lee (d. 1973)Gisele Bündchen (b. 1980) More anniversaries: July 19 July 20 July 21 Archive By email List of days of the year About C/2022 E3 (ZTF) is a non-periodic comet from the Oort cloud that was discovered by the Zwicky Transient Facility (ZTF) in 2022. With a comet nucleus of around 1 kilometre (0.62 mi) in diameter, C/2022 E3 rotates on its axis once every 8.5 hours. It has a cyan coma and dust and gas extended for millions of kilometres, and through the last 10 years a dust tail and ion tail. Its closest approach to the Sun, or perihelion, was on 12 January 2023, and a closest approach to Earth was on 1 February 2023, at a distance of 0.28 AU (42 million km; 26 million mi). The comet reached magnitude 5 in February 2023 and was visible with the naked eye under moonless dark skies. This photograph of C/2022 E3 was taken in January 2023 and released by the Italian National Institute for Astrophysics. Photograph credit: Alessandro Bianconi; National Institute for Astrophysics Recently featured: Passion fruit Basilica of St Paul, Rabat Clouded Apollo Archive More featured pictures Community portal – The central hub for editors, with resources, links, tasks, and announcements. Village pump – Forum for discussions about Wikipedia itself, including policies and technical issues. Site news – Sources of news about Wikipedia and the broader Wikimedia movement. Teahouse – Ask basic questions about using or editing Wikipedia. Help desk – Ask questions about using or editing Wikipedia. Reference desk – Ask research questions about encyclopedic topics. Content portals – A unique way to navigate the encyclopedia. Wikipedia is written by volunteer editors and hosted by the Wikimedia Foundation, a non-profit organization that also hosts a range of other volunteer projects: CommonsFree media repository MediaWikiWiki software development Meta-WikiWikimedia project coordination WikibooksFree textbooks and manuals WikidataFree knowledge base WikinewsFree-content news WikiquoteCollection of quotations WikisourceFree-content library WikispeciesDirectory of species WikiversityFree learning tools WikivoyageFree travel guide WiktionaryDictionary and thesaurus This Wikipedia is written in English. Many other Wikipedias are available; some of the largest are listed below. 1,000,000+ articles العربية Deutsch Español فارسی Français Italiano Nederlands 日本語 Polski Português Русский Svenska Українська Tiếng Việt 中文 250,000+ articles Bahasa Indonesia Bahasa Melayu Bân-lâm-gú Български Català Čeština Dansk Eesti Ελληνικά Esperanto Euskara עברית Հայերեն Magyar Norsk bokmål Română Simple English Slovenčina Srpski Srpskohrvatski Suomi Türkçe Oʻzbek 50,000+ articles Asturianu Azərbaycanca [illegible] Bosanski کوردی Frysk Gaeilge Galego Hrvatski ქართული Kurdî Latviešu Lietuvių [illegible] Македонски [illegible] Norsk nynorsk [illegible] Shqip Slovenščina [illegible] اردو Retrieved from " 2This article needs additional citations for verification. Please help improve this article by adding citations to reliable sources. Unsourced material may be challenged and removed. Find sources: "1807" – news · newspapers · books · scholar · JSTOR (November 2015) (Learn how and when to remove this message) Calendar year Years Millennium 2nd millennium Centuries 18th century 19th century 20th century Decades 1780s 1790s 1800s 1810s 1820s Years 1804 1805 1806 1807 1808 1809 1810 vte February 7: Napoleon leads French troops into Russia in winter, and fights the Battle of Eylau. June 14: Napoleon triumphs over Russia's General Bennigsen, at the Battle of Friedland. 1807 (MDCCCVII) was a common year starting on Thursday of the Gregorian calendar and a common year starting on Tuesday of the Julian calendar, the 1807th year of the Common Era (CE) and Anno Domini (AD) designations, the 807th year of the 2nd millennium, the 7th year of the 19th century, and the 8th year of the 1800s decade. As of the start of 1807, the Gregorian calendar was 12 days ahead of the Julian calendar, which remained in localized use until 1923. Calendar year 1807 by topic Humanities Archaeology Architecture Art Literature Poetry Music By country Australia Brazil Canada Denmark France Germany New Zealand Norway Russia South Africa Sweden United Kingdom United States Other topics Rail transport Science Sports Lists of leaders Sovereign state leaders Territorial governors Religious leaders Law Birth and death categories Births Deaths Establishments and disestablishments categories Establishments Disestablishments Works category Works vte 1807 in various calendarsGregorian calendar1807MDCCCVIIAb urbe condita2560Armenian calendar1256ԹՌԾԶAssyrian calendar6557Balinese saka calendar1728–1729Bengali calendar1213–1214Berber calendar2757British Regnal year47 Geo. 3 – 48 Geo. 3Buddhist calendar2351Burmese calendar1169Byzantine calendar7315–7316Chinese calendar丙寅年 (Fire Tiger)4504 or 4297 — to — 丁卯年 (Fire Rabbit)4505 or 4298Coptic calendar1523–1524Discordian calendar2973Ethiopian calendar1799–1800Hebrew calendar5567–5568Hindu calendars - Vikram Samvat1863–1864 - Shaka Samvat1728–1729 - Kali Yuga4907–4908Holocene calendar11807Igbo calendar807–808Iranian calendar1185–1186Islamic calendar1221–1222Japanese calendarBunka 4 (文化４年)Javanese calendar1733–1734Julian calendarGregorian minus 12 daysKorean calendar4140Minguo calendar105 before ROC民前105年Nanakshahi calendar339Thai solar calendar2349–2350Tibetan calendar[illegible] (male Fire-Tiger)1933 or 1552 or 780 — to — [illegible] (female Fire-Rabbit)1934 or 1553 or 781 Wikimedia Commons has media related to 1807. January 7 – The United Kingdom of Great Britain and Ireland issues an Order in Council prohibiting British ships from trading with France or its allies.[1] January 20 – The Sierra Leone Company, faced with bankruptcy because of the abolition of the slave trade in British colonies, petitions the British government for purchase and transfer of the colony to the Crown; Parliament approves the transfer to take effect on January 1, 1808. [2] February 3 – Napoleonic Wars and Anglo-Spanish War: Battle of Montevideo – The British Army captures Montevideo from the Spanish Empire, as part of the British invasions of the Río de la Plata. February 7 – Napoleon leads the forces of the French Empire in an invasion of the Russian Empire, and begins fighting at the Battle of Eylau against Russian and Prussian forces.[3] February 8 – Battle of Eylau: Napoleon fights a hard but inconclusive battle against the Russians under Bennigsen. February 10 – The Survey of the Coast (renamed the United States Coast Survey in 1836 and the United States Coast and Geodetic Survey in 1878) is established; work begins on August 3, 1816. February 17 – Henry Christophe is elected first President of the State of Haiti, ruling the northern part of the country. February 19 – Burr conspiracy: In Alabama, former Vice President of the United States Aaron Burr is arrested for treason, and confined to Fort Stoddert. February 23 – The Slave Trade Act is passed in the House of Commons of the United Kingdom by an overwhelming majority.[4] March 2 – The United States Congress passes the Act Prohibiting Importation of Slaves "into any port or place within the jurisdiction of the United States ... from any foreign kingdom, place, or country" (to take effect January 1, 1808). March 25 – The Slave Trade Act becomes law, abolishing the slave trade in most of the British Empire[5] with effect from 1 May (slavery itself is abolished in British colonies in 1833). The Swansea and Mumbles Railway in South Wales, at this time known as the Oystermouth Railway, becomes the first passenger-carrying railway in the world. March 29 – H. W. Olbers discovers the asteroid Vesta. April 4–12 – Froberg mutiny: The British troops mutiny at Fort Ricasoli, Malta, by men of the irregularly-recruited Froberg Regiment. April 14 – African Institution holds its first meeting in London; it is intended to improve social conditions in Sierra Leone. May 22 – A grand jury indicts former Vice President of the United States Aaron Burr for treason.[6] May 24 – Siege of Danzig ends after 6 weeks with Prussian and Russian defenders capitulating to French forces. May 29 – Selim III, Ottoman Emperor since 1789, is deposed in favour of his nephew Mustafa IV. May 31 – Primitive Methodism originates in an All Day of Prayer at Mow Cop, in the north Midlands of England.[7] June 9 – The Duke of Portland is chosen as Prime Minister after the United Kingdom general election. June 10 – The Battle of Heilsberg ends in a draw. June 14 – Battle of Friedland: Napoleon decisively defeats Bennigsen's Russian army. June 22 – Chesapeake–Leopard affair: British fourth rate HMS Leopard attacks and boards USS Chesapeake off Norfolk, Virginia, seeking deserters. This act of British aggression plays a role in the run-up to the War of 1812. July 5 – A disastrous British attack is mounted against Buenos Aires, during the second failed invasion of the Río de la Plata. July 7–9 – The Treaties of Tilsit are signed between France, Prussia and Russia. Russian Emperor Alexander I ally together against the British. The Prussians are forced to cede more than half their territory, which is formed into the Duchy of Warsaw in their former Polish lands, and the Kingdom of Westphalia in western Germany. The Free City of Danzig is also formed (established September 9 by Napoleon). July 13 – With the death of Henry Benedict Stuart, the last Stuart claimant to the throne of the United Kingdom, Jacobitism comes to an effective end. July 20 – Nicéphore Niépce is awarded a patent by Napoleon Bonaparte for the Pyréolophore, the world's first internal combustion engine, after it successfully powers a boat upstream on the river Saône in France. August 17 – The North River Steamboat, Robert Fulton's first American steamboat, leaves New York City for Albany on the Hudson River, inaugurating the first commercial steamboat service in the world. September 1 – Former U.S. Vice President Aaron Burr is acquitted of treason, having been accused of plotting to annex parts of Louisiana and Mexico, to become part of an independent republic. September 2–7 – Battle of Copenhagen: The British Royal Navy bombards Copenhagen with fire bombs and phosphorus rockets, to prevent the Dano-Norwegian navy from surrendering to Napoleon; 30% of the city is destroyed, and 2,000 citizens are killed. September 7 – Robert Morrison, the first Protestant missionary to China, arrives in Guangzhou (Canton).[8] September 13 – Beethoven's Mass in C major, Op. 86, is premiered, commissioned by Nikolaus II, Prince Esterházy, and displeasing him.[9] September 27 – Napoleon purchases the Borghese art collection, including the Antinous Mondragone, and brings it to Paris.[10] October 9 – Prussian Reform Movement: Serfdom is abolished by the October edict. October 13 – The Geological Society of London is founded. October 30 – El Escorial Conspiracy: Ferdinand, Prince of Asturias is arrested for conspiring against his father Charles IV of Spain. November 24 – Battle of Abrantes, Portugal: The French under Jean-Andoche Junot take the town. November 29 – Portuguese Queen Maria I and the Court embark at Lisbon, bound for Brazil. Rio de Janeiro becomes the Portuguese capital. December 5–11 – Napoleonic Wars: Raid on Griessie – A British Royal Navy squadron attacks the Dutch port of Griessie on Java in the Dutch East Indies, eliminating the last Dutch naval force in the Pacific and concluding the Java campaign of 1806–1807. [11] December 17 – Napoleonic Wars: France issues the Milan Decree which confirms the Continental System (i.e. no European country is to trade with the United Kingdom). December 22 – The United States Congress passes the Embargo Act, a trade embargo on all foreign nations. Battle of Hingakaka between two factions of Māori people, the largest battle ever fought in New Zealand, and the last fought there without firearms.[12] In 1807 or 1808 is fought the Battle of Moremonui, first of the Musket Wars. Robert E. Lee January 13 – Napoleon Bonaparte Buford, American general, railroad executive (d. 1883) January 19 – Robert E. Lee, American Confederate general (d. 1870) January 28 – Robert McClure, Irish-born Arctic explorer (d. 1873) February 10 – Lajos Batthyány, 1st Prime Minister of Hungary (d. 1849) February 27 – Henry Wadsworth Longfellow, American poet (d. 1882)[13] March 1 – Wilford Woodruff, American religious leader (d. 1898) March 14 – Josephine of Leuchtenberg, Queen of Sweden and Norway (d. 1876) April 2 – William F. Packer, American politician (d. 1870) April 3 – Jane Digby, English adventurer (d. 1881) April 20 – Aloysius Bertrand, French poet (d. 1841) April 24 – Adrien-François Servais, Belgian musician (d. 1866) June 10 – John Westcott, American surveyor and politician (d. 1888) Giuseppe Garibaldi July 4 – Giuseppe Garibaldi, Italian patriot (d. 1882) August 11 – David Rice Atchison, American politician (d. 1886) August 15 – Jules Grévy, 4th President of France (d. 1891) August 18 – Charles Francis Adams Sr., American historical editor, politician and diplomat (d. 1886) September 2 – Fredrika Runeberg, Finnish writer (d. 1879)[14] September 7 – Henry Sewell, 1st Premier of New Zealand (d. 1879) September 16 – John Lenthall, American naval architect and shipbuilder (d. 1882) October 8 – Harriet Taylor, English philosophical writer (d. 1858)[15] October 26 – Barbu Catargiu, 1st Prime Minister of Romania (d. 1862) October 28 – Andrea Kraljević, Herzegovinian Catholic bishop (d. 1879) October 30 – Christopher Wordsworth, Bishop of Lincoln (d. 1885) November 16 – Jean-Pierre Elie Lalande, French astronomer (d. 1732) December 8 – Friedrich Traugott Kützing, German pharmacist, botanist and phycologist (d. 1893) December 17 – John Greenleaf Whittier, American Quaker poet and abolitionist (d. 1892) Pasquale Paoli February 1 – Sir Thomas Troubridge, 1st Baronet, British admiral (b. c. 1758) February 5 – Pasquale Paoli, Corsican patriot, military leader (b. 1725) February 27 – Louise du Pierry, French astronomer (b.1746) March 10 – Jean Puget, French soldier (b. 1698) April 4 – Jérôme Lalande, French astronomer (b. 1732) April 10 – Duchess Anna Amalia of Brunswick-Wolfenbüttel, regent of Weimar and Eisenach (b. 1739) May 10 – Jean-Baptiste Donatien de Vimeur, comte de Rochambeau, French soldier (b. 1725) May 17 – John Gunby, Maryland soldier in the American Revolutionary War (b. 1745) May 18 – John Douglas, Scottish Anglican bishop, man of letters (b. 1721) June 9 – Andrew Sterett, American naval officer (b. 1778) July 13 – Henry Benedict Stuart, Jacobite claimant to the British throne (b. 1725) July 29 – Uriah Tracy, American politician and congressman from Connecticut, 1793 until 1807 (b. 1755) September 16 – George Townshend, 1st Marquess Townshend, British field marshal (b. 1724) October 22 – Jean-François Houbigant, French perfumer (b. 1752) November 2 – Louis Auguste Le Tonnelier de Breteuil, Prime Minister of King Louis XVI of France (b. 1730) November 5 – Angelica Kauffman, Swiss painter (b. 1741) November 8 – Darejan Dadiani, Georgian queen consort (b. 1738) Pierre-Alexandre-Laurent Forfait, French engineer, hydrographer, politician, and Minister of the Navy (1799–1801) (b. 1752) November 23 – Jean-François Rewbell, French politician (b. 1747) November 26 – Oliver Ellsworth, American politician and 3rd Chief Justice of the United States Supreme Court (b. 1745) December 19 – Friedrich Melchior, Baron von Grimm, German writer (b. 1723) December 21 – John Newton, English cleric, hymnist (b. 1725) December 29 – Diogo de Carvalho e Sampayo, Portuguese diplomat, scientist (b. 1750) ^ William S. Dudley, ed. The Naval War of 1812: A Documentary History (Naval Historical Center, 1985) p34 ^ Stephen Tomkins, The Clapham Sect: How Wilberforce's Circle Transformed Britain (Lion Books, 2012) p200 ^ William Hodgson, The Life of Napoleon Bonaparte, Once Emperor of the French, Who Died in Exile, at St. Helena, After a Captivity of Six Years' Duration (Orlando Hodgson, 1841) p384 ^ "William Wilberforce (1759–1833)". Retrieved January 18, 2021. ^ "Abolition of the Slave Trade 1807". BBC. Archived from the original on October 11, 2007. Retrieved September 13, 2007. ^ "Burr Trial - Aaron Burr Treason Trial" (PDF). ^ Farndale, W. E. (1950). The Secret of Mow Cop: a new appraisal of the origins of Primitive Methodism. London: Epworth Press. ^ "Sketch of the Canton Protestant Mission", by Rev. John Chalmers, in The Chinese Recorder and Missionary Journal, Volume 7 (American Presbyterian Mission Press, 1876) p174 ^ Marston, Nicholas (2006). Beethoven: Mass in C major, Op. 86 (PDF) (CD). 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"Mill [née Hardy; other married name Taylor], Harriet". Oxford Dictionary of National Biography (online ed.). Oxford University Press. doi:10.1093/ref:odnb/38051. (Subscription or UK public library membership required.) Retrieved from " 2Second-largest asteroid This article is about the asteroid. For the Roman goddess, see Vesta (mythology). For other uses, see Vesta (disambiguation). 4 VestaTrue color image of Vesta taken by Dawn. The massive Rheasilvia crater dominates Vesta's south pole.DiscoveryDiscovered byHeinrich Wilhelm OlbersDiscovery date29 March 1807DesignationsMPC designation(4) VestaPronunciation/ˈvɛstə/[1]Named afterVestaMinor planet categoryMain belt (Vesta family)AdjectivesVestanVestian[2]Symbol (historically astronomical, now astrological)Orbital characteristics[6]Epoch 13 September 2023(JD 2453300.5)Aphelion2.57 AU (384 million km)Perihelion2.15 AU (322 million km)Semi-major axis2.36 AU (353 million km)Eccentricity0.0894Orbital period (sidereal)3.63 yr (1325.86 d)Average orbital speed19.34 km/sMean anomaly169.4°Inclination7.1422° to ecliptic5.58° to invariable plane[7]Longitude of ascending node103.71°Time of perihelion26 December 2021[8]Argument of perihelion151.66°Satellites NoneEarth MOID1.14 AU (171 million km)Proper orbital elements[9]Proper semi-major axis2.36151 AUProper eccentricity0.098758Proper inclination6.39234°Proper mean motion99.1888 deg / yrProper orbital period3.62944 yr (1325.654 d)Precession of perihelion36.8729 arcsec / yrPrecession of the ascending node−39.5979 (2182 years) arcsec / yrPhysical characteristicsDimensions572.6 km × 557.2 km × 446.4 km[10]Mean diameter525.4±0.2 km[10]Flattening0.2204Surface area(8.66±0.2)×105 km2[b][11]Volume7.4970×107 km3[10]Mass2.590271±0.000058)×1020 kg[12]Mean density3.456±0.035 g/cm3[10]Equatorial surface gravity0.22 m/s2 (0.022 g0)Equatorial escape velocity0.36 km/sSynodic rotation period0.2226 d (5.342 h)[6][13]Equatorial rotation velocity93.1 m/s[c]Axial tilt29°North pole right ascension20h 32m[d]North pole declination48°[d]Geometric albedo0.423[15]Temperature: 75 K (−198 °C)max: 250 K (−23 °C)[16]Spectral typeV[6][17]Apparent magnitude5.1[18] to 8.48Absolute magnitude (H)3.20[6][15]Angular diameter0.70" to 0.22" Vesta (minor-planet designation: 4 Vesta) is one of the largest objects in the asteroid belt, with a mean diameter of 525 kilometres (326 mi).[10] It was discovered by the German astronomer Heinrich Wilhelm Matthias Olbers on 29 March 1807[6] and is named after Vesta, the virgin goddess of home and hearth from Roman mythology.[19] Vesta is thought to be the second-largest asteroid, both by mass and by volume, after the dwarf planet Ceres,[20][21][22] and it is 25% to 30% more massive than any other asteroid. It constitutes an estimated 9% of the mass of the asteroid belt.[23] Vesta is the only known remaining rocky protoplanet of the kind that formed the terrestrial planets.[24] Numerous fragments of Vesta were ejected by collisions one and two billion years ago that left two enormous craters occupying much of Vesta's southern hemisphere.[25][26] Debris from these events has fallen to Earth as howardite–eucrite–diogenite (HED) meteorites, which have been a rich source of information about Vesta.[27][28][29] Vesta is the brightest asteroid visible from Earth. It is regularly as bright as magnitude 5.1,[18] at which times it is faintly visible to the naked eye. Its maximum distance from the Sun is slightly greater than the minimum distance of Ceres from the Sun,[e] although its orbit lies entirely within that of Ceres.[30] NASA's Dawn spacecraft entered orbit around Vesta on 16 July 2011 for a one-year exploration and left the orbit of Vesta on 5 September 2012[31] en route to its final destination, Ceres. Researchers continue to examine data collected by Dawn for additional insights into the formation and history of Vesta.[32][33] Vesta, Ceres, and the Moon with sizes shown to scale Heinrich Olbers discovered Pallas in 1802, the year after the discovery of Ceres. He proposed that the two objects were the remnants of a destroyed planet. He sent a letter with his proposal to the British astronomer William Herschel, suggesting that a search near the locations where the orbits of Ceres and Pallas intersected might reveal more fragments. These orbital intersections were located in the constellations of Cetus and Virgo.[34] Olbers commenced his search in 1802, and on 29 March 1807 he discovered Vesta in the constellation Virgo—a coincidence, because Ceres, Pallas, and Vesta are not fragments of a larger body. Because the asteroid Juno had been discovered in 1804, this made Vesta the fourth object to be identified in the region that is now known as the asteroid belt. The discovery was announced in a letter addressed to German astronomer Johann H. Schröter dated 31 March.[35] Because Olbers already had credit for discovering a planet (Pallas; at the time, the asteroids were considered to be planets), he gave the honor of naming his new discovery to German mathematician Carl Friedrich Gauss, whose orbital calculations had enabled astronomers to confirm the existence of Ceres, the first asteroid, and who had computed the orbit of the new planet in the remarkably short time of 10 hours.[36][37] Gauss decided on the Roman virgin goddess of home and hearth, Vesta.[38] Vesta was the fourth asteroid to be discovered, hence the number 4 in its formal designation. The name Vesta, or national variants thereof, is in international use with two exceptions: Greece and China. In Greek, the name adopted was the Hellenic equivalent of Vesta, Hestia (4 Εστία); in English, that name is used for 46 Hestia (Greeks use the name "Hestia" for both, with the minor-planet numbers used for disambiguation). In Chinese, Vesta is called the 'hearth-god(dess) star', 灶神星 Zàoshénxīng, naming the asteroid for Vesta's role, similar to the Chinese names of Uranus, Neptune, and Pluto.[f] Upon its discovery, Vesta was, like Ceres, Pallas, and Juno before it, classified as a planet and given a planetary symbol. The symbol represented the altar of Vesta with its sacred fire and was designed by Gauss.[39][40] In Gauss's conception, now obsolete, this was drawn . His form is in the pipeline for Unicode 17.0 as U+1F777 .[41][g] The asteroid symbols were gradually retired from astronomical use after 1852, but the symbols for the first four asteroids were resurrected for astrology in the 1970s. The abbreviated modern astrological variant of the Vesta symbol is (U+26B6 ⚶).[41][h] After the discovery of Vesta, no further objects were discovered for 38 years, and during this time the Solar System was thought to have eleven planets.[47] However, in 1845, new asteroids started being discovered at a rapid pace, and by 1851 there were fifteen, each with its own symbol, in addition to the eight major planets (Neptune had been discovered in 1846). It soon became clear that it would be impractical to continue inventing new planetary symbols indefinitely, and some of the existing ones proved difficult to draw quickly. That year, the problem was addressed by Benjamin Apthorp Gould, who suggested numbering asteroids in their order of discovery, and placing this number in a disk (circle) as the generic symbol of an asteroid. Thus, the fourth asteroid, Vesta, acquired the generic symbol ④. This was soon coupled with the name into an official number–name designation, ④ Vesta, as the number of minor planets increased. By 1858, the circle had been simplified to parentheses, (4) Vesta, which were easier to typeset. Other punctuation, such as 4) Vesta and 4, Vesta, was also briefly used, but had more or less completely died out by 1949.[48] SPHERE image is shown on the left, with a synthetic view derived from Dawn images shown on the right for comparison.[49] Photometric observations of Vesta were made at the Harvard College Observatory in 1880–1882 and at the Observatoire de Toulouse in 1909. These and other observations allowed the rotation rate of Vesta to be determined by the 1950s. However, the early estimates of the rotation rate came into question because the light curve included variations in both shape and albedo.[50] Early estimates of the diameter of Vesta ranged from 383 kilometres (238 mi) in 1825, to 444 km (276 mi). E.C. Pickering produced an estimated diameter of 513 ± 17 km (319 ± 11 mi) in 1879, which is close to the modern value for the mean diameter, but the subsequent estimates ranged from a low of 390 km (242 mi) up to a high of 602 km (374 mi) during the next century. The measured estimates were based on photometry. In 1989, speckle interferometry was used to measure a dimension that varied between 498 and 548 km (309 and 341 mi) during the rotational period.[51] In 1991, an occultation of the star SAO 93228 by Vesta was observed from multiple locations in the eastern United States and Canada. Based on observations from 14 different sites, the best fit to the data was an elliptical profile with dimensions of about 550 km × 462 km (342 mi × 287 mi).[52] Dawn confirmed this measurement.[i] These measurements will help determine the thermal history, size of the core, role of water in asteroid evolution and what meteorites found on Earth come from these bodies, with the ultimate goal of understanding the conditions and processes present at the solar system's earliest epoch and the role of water content and size in planetary evolution.[53] Vesta became the first asteroid to have its mass determined. Every 18 years, the asteroid 197 Arete approaches within 0.04 AU of Vesta. In 1966, based upon observations of Vesta's gravitational perturbations of Arete, Hans G. Hertz estimated the mass of Vesta at (1.20±0.08)×10−10 M☉ (solar masses).[54] More refined estimates followed, and in 2001 the perturbations of 17 Thetis were used to calculate the mass of Vesta to be (1.31±0.02)×10−10 M☉.[55] Dawn determined it to be 1.3029×10−10 M☉. Vesta orbits the Sun between Mars and Jupiter, within the asteroid belt, with a period of 3.6 Earth years,[6] specifically in the inner asteroid belt, interior to the Kirkwood gap at 2.50 AU. Its orbit is moderately inclined (i = 7.1°, compared to 7° for Mercury and 17° for Pluto) and moderately eccentric (e = 0.09, about the same as for Mars).[6] True orbital resonances between asteroids are considered unlikely. Because of their small masses relative to their large separations, such relationships should be very rare.[56] Nevertheless, Vesta is able to capture other asteroids into temporary 1:1 resonant orbital relationships (for periods up to 2 million years or more) and about forty such objects have been identified.[57] Decameter-sized objects detected in the vicinity of Vesta by Dawn may be such quasi-satellites rather than proper satellites.[57] Olbers Regio (dark area) defines the prime meridian in the IAU coordinate system. It is shown here in a Hubble shot of Vesta, because the crater Claudia (indicated by the arrow at the bottom of the closeup image at right), which defines the prime meridian in the Dawn/NASA coordinate system, is only 700 m across. Vesta's rotation is relatively fast for an asteroid (5.342 h) and prograde, with the north pole pointing in the direction of right ascension 20 h 32 min, declination +48° (in the constellation Cygnus) with an uncertainty of about 10°. This gives an axial tilt of 29°.[58] Two longitudinal coordinate systems are used for Vesta, with prime meridians separated by 150°. The IAU established a coordinate system in 1997 based on Hubble photos, with the prime meridian running through the center of Olbers Regio, a dark feature 200 km across. When Dawn arrived at Vesta, mission scientists found that the location of the pole assumed by the IAU was off by 10°, so that the IAU coordinate system drifted across the surface of Vesta at 0.06° per year, and also that Olbers Regio was not discernible from up close, and so was not adequate to define the prime meridian with the precision they needed. They corrected the pole, but also established a new prime meridian 4° from the center of Claudia, a sharply defined crater 700 metres across, which they say results in a more logical set of mapping quadrangles.[59] All NASA publications, including images and maps of Vesta, use the Claudian meridian, which is unacceptable to the IAU. The IAU Working Group on Cartographic Coordinates and Rotational Elements recommended a coordinate system, correcting the pole but rotating the Claudian longitude by 150° to coincide with Olbers Regio.[60] It was accepted by the IAU, although it disrupts the maps prepared by the Dawn team, which had been positioned so they would not bisect any major surface features.[59][61] Relative sizes of the four largest asteroids. Vesta is second from left. This graph was using the legacy Graph extension, which is no longer supported. It needs to be converted to the new Chart extension.The mass of 4 Vesta (blue) compared to other large asteroids: 1 Ceres, 2 Pallas, 10 Hygiea, 704 Interamnia, 15 Eunomia and the remainder of the Main Belt. The unit of mass is ×1018 kg. Other objects in the Solar System with well-defined masses within a factor of 2 of Vesta's mass are Varda, Gǃkúnǁʼhòmdímà, and Salacia (245, 136, and 492×1018 kg, respectively). No moons are in this range: the closest, Tethys (Saturn III) and Enceladus (Saturn II), are over twice and less than half of Vesta's mass. Vesta is the second most massive body in the asteroid belt, though it is only 28% as massive as Ceres, the largest.[9][23][62][23] Vesta is, however, the most massive body that formed in the asteroid belt, as Ceres is believed to have formed between Jupiter and Saturn. Vesta's density is lower than those of the four terrestrial planets but is higher than those of most asteroids, as well as all of the moons in the Solar System except Io. Vesta's surface area is about the same as the land area of Pakistan, Venezuela, Tanzania, or Nigeria; slightly under 900,000 km2 (350,000 sq mi; 90 million ha; 220 million acres). It has an only partially differentiated interior.[63] Vesta is only slightly larger (525.4±0.2 km[10]) than 2 Pallas (512±3 km) in mean diameter,[64] but is about 25% more massive. Vesta's shape is close to a gravitationally relaxed oblate spheroid,[58] but the large concavity and protrusion at the pole (see 'Surface features' below) combined with a mass less than 5×1020 kg precluded Vesta from automatically being considered a dwarf planet under International Astronomical Union (IAU) Resolution XXVI 5.[65] A 2012 analysis of Vesta's shape[66] and gravity field using data gathered by the Dawn spacecraft has shown that Vesta is currently not in hydrostatic equilibrium.[10][67] Temperatures on the surface have been estimated to lie between about −20 °C (253 K) with the Sun overhead, dropping to about −190 °C (83.1 K) at the winter pole. Typical daytime and nighttime temperatures are −60 °C (213 K) and −130 °C (143 K), respectively. This estimate is for 6 May 1996, very close to perihelion, although details vary somewhat with the seasons.[16] Further information: List of geological features on Vesta Before the arrival of the Dawn spacecraft, some Vestan surface features had already been resolved using the Hubble Space Telescope and ground-based telescopes (e.g., the Keck Observatory).[68] The arrival of Dawn in July 2011 revealed the complex surface of Vesta in detail.[69] Geologic map of Vesta (Mollweide projection).[70] The most ancient and heavily cratered regions are brown; areas modified by the Veneneia and Rheasilvia impacts are purple (the Saturnalia Fossae Formation, in the north)[70] and light cyan (the Divalia Fossae Formation, equatorial),[70] respectively; the Rheasilvia impact basin interior (in the south) is dark blue, and neighboring areas of Rheasilvia ejecta (including an area within Veneneia) are light purple-blue;[71][72] areas modified by more recent impacts or mass wasting are yellow/orange or green, respectively. Main articles: Rheasilvia and Veneneia Northern (left) and southern (right) hemispheres. The "Snowman" craters are at the top of the left image; Rheasilvia and Veneneia (green and blue) dominate the right. Parallel troughs are seen in both. Colors of the two hemispheres are not to scale,[j] and the equatorial region is not shown. South pole of Vesta, showing the extent of Rheasilvia crater. The most prominent surface features are two enormous impact basins, the 500-kilometre-wide (311 mi) Rheasilvia, centered near the south pole; and the 400-kilometre-wide (249 mi) Veneneia. The Rheasilvia impact basin is younger and overlies the Veneneia.[74] The Dawn science team named the younger, more prominent crater Rheasilvia, after the mother of Romulus and Remus and a mythical vestal virgin.[75] Its width is 95% of the mean diameter of Vesta. The crater is about 19 km (12 mi) deep. A central peak rises 23 km (14 mi) above the lowest measured part of the crater floor and the highest measured part of the crater rim is 31 km (19 mi) above the crater floor low point. It is estimated that the impact responsible excavated about 1% of the volume of Vesta, and it is likely that the Vesta family and V-type asteroids are the products of this collision. If this is the case, then the fact that 10 km (6 mi) fragments have survived bombardment until the present indicates that the crater is at most only about 1 billion years old.[76] It would also be the site of origin of the HED meteorites. All the known V-type asteroids taken together account for only about 6% of the ejected volume, with the rest presumably either in small fragments, ejected by approaching the 3:1 Kirkwood gap, or perturbed away by the Yarkovsky effect or radiation pressure. Spectroscopic analyses of the Hubble images have shown that this crater has penetrated deep through several distinct layers of the crust, and possibly into the mantle, as indicated by spectral signatures of olivine.[58] Subsequent analysis of data from the Dawn mission provided much greater detail in Rheasilvia's structure, confirming it as one of the largest impact structures in the Solar System relative to its parent body size. [74] The impact clearly modified the pre-existing very large, Veneneia structure, indicating Rheasilvia's younger age.[74] Rheasilvia's size makes Vesta's southern topography unique, creating a flattened southern hemisphere and contributing significantly to the asteroid's overall oblate shape.[69] Rheasilvia's ~22 km (14 mi) central peak stands as one of the tallest mountains identified in the Solar System.[74] Its base width of roughly 180 km (110 mi) and complex morphology distinguishes it from the simpler central peaks seen in smaller craters.[74] Numerical modeling indicates that such a large central structure within a ~505 km (314 mi) diameter basin requires formation on a differentiated body with a relatively weak interior.[77] Scaling laws for craters on smaller asteroids fail to predict such a feature; instead, impact dynamics involving transient crater collapse and rebound of the underlying material (potentially upper mantle) are needed to explain its formation.[77] Hydrocode simulations suggest the impactor responsible was likely 60–70 km (37–43 mi) across, impacting at roughly 5.4 km/s.[78] Models of impact angle (around 30-45 degrees from vertical) better match the detailed morphology of the basin and its prominent peak.[77] Crater density measurements on Rheasilvia's relatively unmodified floor materials and surrounding ejecta deposits, calibrated using standard lunar chronology functions adapted for Vesta's location, place the impact event at approximately 1 billion years ago.[79][70] This makes Rheasilvia a relatively young feature on a protoplanetary body formed early in Solar System history. The estimated excavation of ~1% of Vesta's volume[74] provides a direct link to the Vesta family of asteroids (Vestoids) and the HED meteorites. Since Vesta's spectral signature matches that of the Vestoids and HEDs, this strongly indicates they are fragments ejected from Vesta most likely during the Rheasilvia impact.[27][79] The Dawn mission's VIR instrument helped to connect the basin's deep excavation and compositional diversity. VIR mapping revealed spectral variations across the basin consistent with the mixing of different crustal layers expected in the HED meteorites. Signatures matching eucrites (shallow crustal basalts) and diogenites (deeper crustal orthopyroxenites) were identified, which suggest the impact penetrated deeper lower crust material, which were first inferred at high by Hubble observations is strongly expected but only tentatively detected in small, distinct outcrops.[81][80] As the dominant mineral expected in Vesta's mantle beneath the HED-like crust,[10] the presence of olivine indicates the Rheasilvia impact penetrated Vesta's entire crust (~20–40 km (12–25 mi) thick in the region) and excavated material from the upper mantle.[81] Furthermore, the global stresses resulting from this massive impact are considered the likely trigger for the formation of the large trough systems, like Divalia Fossa, that encircle Vesta's equatorial region.[82][69] The crater Aelia Feralia Planitia, an old, degraded crater 270 km (170 mi) across, which suggests the surface of Vesta is older than Rheasilvia. The crater Feralia Planitia, shown at right, which is 270 km (170 mi) across.[83] More-recent, sharper craters range up to 158 km (98 mi) Varronilla and 196 km (122 mi) Postumia.[84] Dust fills up some craters, creating so-called dust ponds. They are a phenomenon where pockets of ground-up dust accumulated in depressions on the surface of the body (like craters), contrasting from the Rocky terrain around them.[85] On the surface of Vesta, we have identified both type 1 (formed from impact melt) and type 2 (electrostatically made) dust ponds within 0°–30°N/S, that is, Equatorial region. 10 craters have been identified with such formations.[86] The "snowman craters" are a group of three adjacent craters in Vesta's northern hemisphere. Their official names, from largest to smallest (west to east), are Marcia, Calpurnia, and Minucia. Marcia is the youngest and cross-cuts Calpurnia. Minucia is the oldest.[70] "Snowman" craters by Dawn from 5,200 km (3,200 mi) in 2011Detailed image of the "Snowman" craters The majority of the equatorial region of Vesta is sculpted by a series of parallel troughs designated Divalia Fossae; its longest trough is 10–20 kilometres (6.2–12.4 mi) wide and 465 kilometres (289 mi) long. Despite the fact that Vesta is a one-seventh the size of the Moon, Divalia Fossae dwarfs the Grand Canyon. A second series, inclined to the equator, is found further north. This northern trough system is named Saturnalia Fossae, with its largest trough being roughly 40 km (25 mi) wide and over 370 km (230 mi) long. These troughs are thought to be large-scale graben resulting from the impacts that created Rheasilvia and Veneneia craters, respectively. They are some of the longest chasms in the Solar System, nearly as long as Ithaca Chasma on Tethys. The troughs may be graben that formed after another asteroid collided with Vesta, a process that can happen only in a body that is differentiated,[82] which Vesta may not be fully be. Alternatively, it is proposed that the troughs may be radial sculptures created by secondary cratering from Rheasilvia.[87] A section of Divalia Fossae, with parallel to the north and southA computer-generated view of a portion of Divalia Fossae Compositional information from the visible and infrared spectrometer (VIR), gamma-ray and neutron detector (GRaND), and framing camera (FC), all indicate that the majority of the surface composition of Vesta is consistent with the composition of the howardite, eucrite, and diogenite meteorites.[88][89][90] The Rheasilvia region is richest in diogenite, consistent with the Rheasilvia-forming impact excavating material from deeper within Vesta. The presence of olivine within the Rheasilvia region would also be consistent with excavation of mantle material. However, olivine has only been detected in localized regions of the northern hemisphere, not within Rheasilvia.[32] The origin of this olivine is currently unclear. Though olivine was expected by astronomers to have originated from Vesta's mantle prior to the arrival of the Dawn orbiter, the lack of olivine within the

Rheasilvia and Veneneia impact basins complicates this view. Both impact basins excavated Vestian material down to 60–100 km, far deeper than the expected thickness of ~30–40 km for Vesta's crust. Vesta's crust may be far thicker than expected or the violent impact events that created Rheasilvia and Veneneia may have mixed material enough to obscure olivine from observations. Alternatively, Dawn observations of olivine could instead be due to delivery by olivine-rich impactors, unrelated to Vesta's internal structure.[91] Pitted terrain has been observed in four craters on Vesta: Marcia, Cornelia, Numisia and Licinia.[92] The formation of the pitted terrain is proposed to be degassing of impact-heated volatile-bearing material. Along with the pitted terrain, curvilinear gullies are found in Marcia and Cornelia craters. The curvilinear gullies end in lobate deposits, which are sometimes covered by pitted terrain, and are proposed to form by the transient flow of liquid water after buried deposits of ice were melted by the heat of the impacts.[71] Hydrated materials have also been detected, many of which are associated with areas of dark material.[93] Consequently, dark material is thought to be largely composed of carbonaceous chondrite, which was deposited on the surface by impacts. Carbonaceous chondrites are comparatively rich in mineralogically bound OH.[90] Cut-away schematic of Vestan core, mantle, and crust Eucrite meteorite A large collection of potential samples from Vesta is accessible to scientists, in the form of over 1200 HED meteorites (Vestan achondrites), giving insight into Vesta's geologic history and structure. NASA Infrared Telescope Facility (NASA IRTF) studies of asteroid (237442) 1999 TA10 suggest that it originated from deeper within Vesta than the HED meteorites.[94] Vesta is thought to consist of a metallic iron–nickel core, variously estimated to be 90 km (56 mi)[63] to 220 km (140 mi)[10] in diameter, an overlying rocky olivine mantle, with a surface crust of similar composition to HED meteorites. From the first appearance of calcium–aluminium-rich inclusions (the first solid matter in the Solar System, forming about 4.567 billion years ago), a likely time line is as follows:[95][96][97][98][99] Timeline of the evolution of Vesta 2–3 million years Accretion completed 4–5 million years Complete or almost complete melting due to radioactive decay of 26Al, leading to separation of the metal core 6–7 million years Progressive crystallization of a convecting molten mantle. Convection stopped when about 80% of the material had crystallized Extrusion of the remaining molten material to form the crust, either as basaltic lavas in progressive eruptions, or possibly forming a short-lived magma ocean. The deeper layers of the crust crystallize to form plutonic rocks, whereas older basalts are metamorphosed due to the pressure of newer surface layers. Slow cooling of the interior Vesta is the only known intact asteroid that has been resurfaced in this manner. Because of this, some scientists refer to Vesta as a protoplanet.[100] Composition of the Vestan crust (by depth)[101] A lithified regolith, the source of howardites and brecciated eucrites. Basaltic lava flows, a source of non-cumulate eucrites. Plutonic rocks consisting of pyroxene, pigeonite and plagioclase, the source of cumulate eucrites. Plutonic rocks rich in orthopyroxene with large grain sizes, the source of diogenites. On the basis of the sizes of V-type asteroids (thought to be pieces of Vesta's crust ejected during large impacts), and the depth of Rheasilvia crater (see below), the crust is thought to be roughly 10 kilometres (6 mi) thick.[102] Findings from the Dawn spacecraft have found evidence that the troughs that wrap around Vesta could be graben formed by impact-induced faulting (see Troughs section above), meaning that Vesta has more complex geology than other asteroids. The impacts that created the Rheasilvia and Veneneia craters occurred when Vesta was no longer warm and plastic enough to return to an equilibrium shape, distorting its once rounded shape and prohibiting it from being classified as a dwarf planet today.[citation needed] Vesta's surface is covered by regolith distinct from that found on the Moon or asteroids such as Itokawa. This is because space weathering acts differently. Vesta's surface shows no significant trace of nanophase iron because the impact speeds on Vesta are too low to make rock melting and vaporization an appreciable process. Instead, regolith evolution is dominated by brecciation and subsequent mixing of bright and dark components.[103] The dark component is probably due to the infall of carbonaceous material, whereas the bright component is the original Vesta basaltic soil.[104] Some small Solar System bodies are suspected to be fragments of Vesta caused by impacts. The Vestian asteroids and HED meteorites are examples. The V-type asteroid 1929 Kollaa has been determined to have a composition akin to cumulate eucrite meteorites, indicating its origin deep within Vesta's crust.[28] Vesta is currently one of only eight identified Solar System bodies of which we have physical samples, coming from a number of meteorites suspected to be Vestan fragments. It is estimated that 1 out of 16 meteorites originated from Vesta.[105] The other identified Solar System samples are from Earth itself, meteorites from Mars, meteorites from the Moon, and samples returned from the Moon, the comet Wild 2, and the asteroids 25143 Itokawa, 162173 Ryugu, and 101955 Bennu.[29][k] Animation of Dawn's trajectory from 27 September 2007 to 5 October 2018 Dawn · Earth · Mars · 4 Vesta · 1 Ceres First image of asteroids (Ceres and Vesta) taken from Mars. The image was made by the Curiosity rover on 20 April 2014. Animation of Dawn's trajectory around 4 Vesta from 15 July 2011 to 10 September 2012 Dawn · 4 Vesta In 1981, a proposal for an asteroid mission was submitted to the European Space Agency (ESA). Named the Asteroidal Gravity Optical and Radar Analysis (AGORA), this spacecraft was to launch some time in 1990–1994 and perform two flybys of large asteroids. The preferred target for this mission was Vesta. AGORA would reach the asteroid belt either by a gravitational slingshot trajectory past Mars or by means of a small ion engine. However, the proposal was refused by the ESA. A joint NASA–ESA asteroid mission was then drawn up for a Multiple Asteroid Orbiter with Solar Electric Propulsion (MAOSEP), with one of the mission profiles including an orbit of Vesta. NASA indicated they were not interested in an asteroid mission. Instead, the ESA set up a technological study of a spacecraft with an ion drive. Other missions to the asteroid belt were proposed in the 1980s by France, Germany, Italy and the United States, but none were approved.[106] Exploration of Vesta by fly-by and impacting penetrator was the second main target of the first plan of the multi-aimed Soviet Vesta mission, developed in cooperation with European countries for realisation in 1991–1994 but canceled due to the dissolution of the Soviet Union. Artist's conception of Dawn orbiting Vesta In the early 1990s, NASA initiated the Discovery Program, which was intended to be a series of low-cost scientific missions. In 1996, the program's study team recommended a mission to explore the asteroid belt using a spacecraft with an ion engine as a high priority. Funding for this program remained problematic for several years, but by 2004 the Dawn vehicle had passed its critical design review[107] and construction proceeded.[citation needed] It launched on 27 September 2007 as the first space mission to Vesta. On 3 May 2011, Dawn acquired its first targeting image 1.2 million kilometres (0.75×10^6 mi) from Vesta.[108] On 16 July 2011, NASA confirmed that it received telemetry from Dawn indicating that the spacecraft successfully entered Vesta's orbit.[109] It was scheduled to orbit Vesta for one year, until July 2012.[110] Dawn's arrival coincided with late summer in the southern hemisphere of Vesta, with the large crater at Vesta's south pole (Rheasilvia) in sunlight. Because a season on Vesta lasts eleven months, the northern hemisphere, including anticipated compression fractures opposite the crater, would become visible to Dawn's cameras before it left orbit.[111] Dawn left orbit around Vesta on 4 September 2012 11:26 p.m. PDT to travel to Ceres.[112] NASA/DLR released imagery and summary information from a survey orbit, two high-altitude orbits (60–70 m/pixel) and a low-altitude mapping orbit (20 m/pixel), including digital terrain models, videos and atlases.[113][114][115][116][117][118] Scientists also used Dawn to calculate Vesta's precise mass and gravity field. The subsequent determination of the J2 component yielded a core diameter estimate of about 220 km (140 mi) assuming a crustal density similar to that of the HED.[113] Dawn data can be accessed by the public at the UCLA website.[119] Albedo and spectral maps of 4 Vesta, as determined from Hubble Space Telescope images from November 1994 Elevation map of 4 Vesta, as determined from Hubble Space Telescope images of May 1996 Elevation diagram of 4 Vesta (as determined from Hubble Space Telescope images of May 1996) viewed from the south-east, showing Rheasilvia crater at the south pole and Feralia Planitia near the equator Vesta seen by the Hubble Space Telescope in May 2007 The 2006 IAU draft proposal on the definition of a planet listed Vesta as a candidate.[120] Vesta is shown fourth from the left along the bottom row. Vesta comes into view as the Dawn spacecraft approaches and enters orbit: Vesta from 100,000 km(1 July 2011) Vesta from 41,000 km(9 July 2011) In orbit at 16,000 km(17 July 2011) In orbit from 10,500 km(18 July 2011) The northern hemisphere from 5,200 km(23 July 2011) In orbit from 5,200 km(24 July 2011) In orbit from 3,700 km(31 July 2011) Full rotation(1 August 2011) Composite greyscale image Cratered terrain with hills and ridges(6 August 2011) Densely cratered terrain near terminator(6 August 2011) Vestan craters in various states of degradation, with troughs at bottom(6 August 2011) Hill shaded central mound at the south pole of Vesta(2 February 2015) Detailed images retrieved during the high-altitude (60–70 m/pixel) and low-altitude (~20 m/pixel) mapping orbits are available on the Dawn Mission website of JPL/NASA.[121] Annotated image from Earth's surface in June 2007 with (4) Vesta Its size and unusually bright surface make Vesta the brightest asteroid, and it is occasionally visible to the naked eye from dark skies (without light pollution). In May and June 2007, Vesta reached a peak magnitude of +5.4, the brightest since 1989.[122] At that time, opposition and perihelion were only a few weeks apart.[123] It was brighter still at its 22 June 2018 opposition, reaching a magnitude of +5.3.[124] Less favorable oppositions during late autumn 2008 in the Northern Hemisphere still had Vesta at a magnitude of from +6.5 to +7.3.[125] Even when in conjunction with the Sun, Vesta will have a magnitude around +8.5; thus from a pollution-free sky it can be observed with binoculars even at elongations much smaller than near opposition.[125] In 2010, Vesta reached opposition in the constellation of Leo on the night of 17–18 February, at about magnitude 6.1,[126] a brightness that makes it visible in binocular range but generally not for the naked eye. Under perfect dark sky conditions where all light pollution is absent it might be visible to an experienced observer without the use of a telescope or binoculars. Vesta came to opposition again on 5 August 2011, in the constellation of Capricornus at about magnitude 5.6.[126][127] Vesta was at opposition again on 9 December 2012.[128] According to Sky and Telescope magazine, this year Vesta came within about 6 degrees of 1 Ceres during the winter of 2012 and spring 2013.[129] Vesta orbits the Sun in 3.63 years and Ceres in 4.6 years, so every 17.4 years Vesta overtakes Ceres (the previous overtaking was in April 1996).[129] On 1 December 2012, Vesta had a magnitude of 6.6, but it had decreased to 8.4 by 1 May 2013.[129] Conjunction of Ceres and Vesta near the star Gamma Virginis on 5 July 2014 in the Constellation of Virgo. Ceres and Vesta came within one degree of each other in the night sky in July 2014.[129] 3103 Eger 3551 Verenia 3908 Nyx 4055 Magellan Asteroids in fiction Diogenite Eucrite List of former planets Howardite Vesta family (vestoids) List of tallest mountains in the Solar System ^ Marc Rayman of the JPL Dawn team used "Vestian" (analogous to the Greek cognate Hestian) a few times in 2010 and early 2011 in his Dawn Journal, and the Planetary Society continued to use that form for a few more years.[2] The word had been used elsewhere, e.g. in Tsiolkovsky (1960) The call of the cosmos. However, otherwise the shorter form "Vestan" has been used by JPL.[3] Most modern print sources also use "Vestan".[4][5]Note that the related word "Vestalian" refers to people or things associated with Vesta, such as the vestal virgins, not to Vesta herself. ^ Calculated using the known dimensions assuming an ellipsoid. ^ Calculated using (1) the known rotation period (5.342 h)[6] and (2) the equatorial radius Req (285 km)[10] of the best-fit biaxial ellipsoid to Asteroid 4 Vesta. ^ a b topocentric coordinates computed for the selected location: Greenwich, United Kingdom[14] ^ On 10 February 2009, during Ceres perihelion, Ceres was closer to the Sun than Vesta, because Vesta has an aphelion distance greater than Ceres's perihelion distance. (10 February 2009: Vesta 2.56 AU; Ceres 2.54 AU) ^ 維斯塔 wéisītǎ is the closest Chinese approximation of the Latin pronunciation westa. ^ Some sources contemporaneous to Gauss invented more elaborate forms, such as and .[43][44] A simplification of the latter from c. 1930, ,[45] never caught on. ^ This symbol can be seen in the top of the most elaborate of the earlier forms, . It dates from 1973, at the beginning of astrological interest in asteroids.[46] ^ The data returned will include, for both asteroids, full surface imagery, full surface spectrometric mapping, elemental abundances, topographic profiles, gravity fields, and mapping of remnant magnetism, if any.[53] ^ that is, blue in the north does not mean the same thing as blue in the south. ^ Note that 6 Hebe may be the parent body for H chondrites, one of the most common meteorite types. ^ "Vesta". Dictionary.com Unabridged (Online). n.d. ^ "Search Results". Planetary Society. Archived from the original on 27 July 2020. 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Adaptive optics views of Vesta from Keck Observatory 4 Vesta images at ESA/Hubble Archived 22 January 2009 at the Wayback Machine Dawn at Vesta (NASA press kit on Dawn's operations at Vesta) NASA video Archived 22 April 2021 at the Wayback Machine Vesta atlas 4 Vesta at AstDyS-2, Asteroids—Dynamic Site Ephemeris · Observation prediction · Orbital info · Proper elements · Observational info 4 Vesta at the JPL Small-Body Database Close approach · Discovery · Ephemeris · Orbit viewer · Orbit parameters · Physical parameters Portals: Stars Spaceflight Outer space Science Retrieved from " 4 The following pages link to 4 Vesta External tools (link count transclusion count sorted list) · See help page for transcluding these entries Showing 50 items. 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